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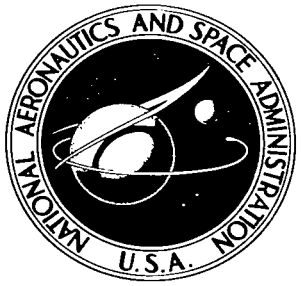

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THE DEVELOPMENT OF A MICROMINIATURE dc SIGNAL-CONDITIONING AMPLIFIER

by Guss E. Wenzel

Manned Spacecraft Center
Houston, Texas

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ABSTRACT

This report details design and development of the basic circuitry for an integrated-circuit direct-coupled amplifier that is stable with respect to time and temperature. The amplifier serves as a basic building block in a microminiature signal-conditioning system.

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THE DEVELOPMENT OF A MICROMINIATURE dc SIGNAL-CONDITIONING AMPLIFIER*

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SUMMARY

The purpose of this effort was to design and develop the basic circuitry for an integrated-circuit, direct-coupled amplifier that is stable with respect to time and temperature. The performance of this amplifier must be either equivalent or superior to a conventional high-performance chopper amplifier. When this development has been completed, the resulting amplifier will serve as a basic building block in a microminiature signal-conditioning system.

The initial phase of this development has been successfully completed. The state of the art of signal-conditioning amplifiers has been definitely extended. It is now feasible to design and develop a space flight signal-conditioning system that will require only 2 to 3 percent of the power, weight, and volume requirements of the present signal-conditioning systems.

This report describes in detail the efforts of the first phase in the amplifier development. In addition to the design and manufacturing considerations, the test results are included. The performance is then compared with the specifications, and comments are made where applicable. Suggestions are proposed for increasing the manufacturing yield and improving the performance.

INTRODUCTION

Several generations of transistorized signal modifiers, built with discrete components, have produced a product that is efficient in power, weight, and volume requirements. The circuit design and packaging techniques have progressed to the stage whereby each generation of modifiers results in only a small improvement. To continue advancing the state of the art for signal-conditioning equipment, action was initiated to organize a development program for an integrated-circuit microminiature signal-conditioning system.

*A portion of this work was performed under Contract NAS 9-3410.

The basic circuit required in the design of a signal-conditioning system is a direct-current (dc) amplifier that is stable with respect to time and temperature. Although direct-coupled amplifiers have been stabilized by numerous methods with various degrees of success, the most successful method of dc amplification has been the chopper amplifier. The chopper amplifier is successful because the signal through the amplifier is an amplitude-modulated square wave and, therefore, can be amplified by resistance-capacitance-coupled stages of gain. This type of design does not amplify the drift in quiescent voltages as does a direct-coupled amplifier. The main disadvantage to the direct-coupled amplifier, built with discrete components, is the problem of maintaining carefully matched temperature-sensitive components at the same temperature. Because of the physical size of these components, it is extremely difficult to maintain an acceptable match. This temperature mismatch, or gradient, will result in a shift in the quiescent points and will appear effectively as a signal. This signal will be amplified then by all of the following stages of gain and will appear at the amplifier output as an error in the signal.

An integrated-circuit amplifier overcomes the temperature-gradient problem of direct-coupled amplifiers that are built with discrete components because all of the components are essentially at the same temperature since the complete circuit is so small. This type of design will be complicated by the lack of potentiometers and similar devices. However, this restriction can be overcome by careful planning of the design.

Several manufacturers have designed and produced a limited number of microminiature dc amplifiers. An analysis of the data of a recently conducted market survey, tabulated in table I, indicates that no company produces an amplifier similar to one which would meet the requirements for use in space flight. These data indicate, and further investigation has confirmed, that an acceptable amplifier can be designed with integrated circuits if a reasonable amount of effort is applied. A detailed description of an integrated dc differential instrumentation amplifier is shown in appendix A.

The dc signal-conditioning amplifier development program is set up to be accomplished in two phases. The first phase is to develop the basic circuitry. Specifications were formulated to reflect typical or worst-case actual flight requirements (appendix B). With this type of amplifier design perfected, it becomes a relatively simple matter to make modifications for the various gain and frequency response requirements for actual flight use. The second phase of the development is to improve the design of the first phase. In a discrete component design, this phase would be neither required nor desired because the circuit design engineer would have sufficient background circuit history to formulate his decisions. However, in advancing the state of the art by using integrated circuits, this background is not available, and the first design may not necessarily be the best design. This phase is considered to be very important because it will allow the circuit design engineer to reconsider the first-phase design. In addition to a reevaluation of the basic design, phase two will help the engineer broaden the specification requirements to insure proper operation in space flight environments and will help to reduce the product cost by allowing consideration of methods for reduction of circuit complexity and of increasing the manufacturing yield.

The packaging of the amplifier does not advance the state of the art. A conventional flat pack was used in the same manner that digital circuits are packaged.

Appendix A of this paper was prepared by David Roy Breuer, TRW Systems Group, Redondo Beach, California.

SYMBOLS

A	open-loop gain exclusive of the input gain stage
A_T	total open-loop gain
A_1, A_2, A_3	gain per stage
CMR	common-mode rejection factor
°C/W	thermal resistance, °C/W
E_R	output bias voltage developed across a resistor R
G_C	common-mode loop gain
I_c	collect current
Q1, Q2, . . . , Qn	transistors
R1, R2, . . . , Rn	resistors
R1A, R1B	resistors used for gain selection
R_E	emitter diffusion resistance of input transistor
R_L	load resistance
R_S	source resistance of input signal
S1	switch
T	loop gain equal to open-loop gain divided by closed-loop gain
V_{BE}	base-emitter voltage
V_{CB}	collector-base voltage
V_{CE}	collector-emitter voltage

V_{CS}	collector-substrate voltage
VR	voltage regulator
v_i	input-signal voltage
v_o	output-signal voltage
$Z_{in(CM)}$	common-mode input impedance
ß	current gain of the input transistors
ΔI_{CBO}	collector-base leakage current difference of the two input transistors

MANUFACTURING CONSIDERATIONS

The most ideal design would be to manufacture the entire amplifier on a single silicon die. However, because of yield purposes, the amplifier was designed by using eight separate dice. Careful division of the circuitry permitted a common transistor substrate, named the multicircuit die (MCD), to be used in providing the different dice at a minimum cost. In figure 1, the mask layout of the MCD with its 12 transistors, 4 circuit crossovers, and 1 test transistor is shown. The MCD is put to practical use with the aid of the four special masks shown in figure 2. These masks are used to vacuum-deposit the resistors and interconnections necessary to produce a specific circuit.

The various dice in relation to the complete amplifier schematic diagram are shown in figure 3. A breakdown of these dice is as follows:

Die	Function	MCD	Transistors	Resistors	Capacitors
RA-01	Resistor array	No	0	9	0
DM-02	Input amplifier	Yes	9	8	0
CA-01	Capacitor array	No	0	0	4
DM-01A	Output amplifier	Yes	12	15	0
VR-02	Voltage regulator	Yes	11	9	0
VR-01	Voltage regulator	Yes	10	9	0
DO-01	Drift offset control	Yes	6	15	0
CM-01	Common-mode amplifier	Yes	6	12	0
8	Complete amplifier	---	54	77	4

The photographic mask layout of these dice and the schematics are presented in figures 4 to 19. An analysis of these drawings shows that some resistors can be adjusted for optimum amplifier performance. The adjustment technique is as follows: the main portion of the resistor is made a few percent smaller than the design value; in series with this resistor are several smaller resistors that are shorted by aluminum fuse links; the exact resistance required for optimum amplifier performance is determined by a test condition; then this value of resistance is obtained by opening the corresponding fuse links with high-current pulses. Figure 20 is a photograph of a fuse link before and after opening. In the same manner, the capacitors are adjustable by a parallel layout.

The previously mentioned eight dice are mounted in a flat package with a high-temperature epoxy (fig. 21). The dice are interconnected and connected to the flat-package leads with the 1.5-mil gold wire as illustrated in figure 22.

The amplifier is energized with power supply voltages and stimulated with an input signal. Various tests are conducted to determine the values of the adjustable resistors and capacitors. After these values are selected, the amplifier is sealed and acceptance-tested.

A summary of the manufacturing sequence is as follows:

1. Manufacture, select, and stockpile MCD wafers; each wafer contains approximately 125 dice.

2. Generate the four photographic masks required to produce a specific circuit and process the wafers.

3. Test and catalog each die. (Each die has a serial number.)

4. Separate and sort the dice.

5. Mount the dice in the flat pack and interconnect with 1.5-mil gold wire.

6. Test and select the adjustable resistors and capacitors.

7. Seal the package and perform acceptance tests.

COMPLIANCE TO SPECIFICATIONS

The specifications for the development of the direct-coupled amplifier are derived from either typical or worst-case actual flight requirements, depending on the component being considered and the conditions to which it will be subjected. With this philosophy as a basis for design, the resultant equipment can be used or easily modified with the assured success of producing amplifiers suitable for future spacecraft applications.

The following paragraphs present a detailed listing of these specifications with suitable comments and actual laboratory test data.

Supply Voltage Conditions

The nominal voltage and current is to be selected by the circuit designer. This voltage may vary by ±5 percent over a frequency range of from dc to 100 kHz.

The intent of this specification is to assure that the circuit design engineer, who would be the best qualified person, would be able to select the supply voltages most desirable for the design. In actuality, the engineer must consider eventually the fact that he cannot have an ideal supply source. For the design effort, the maximum current drain on this supply was omitted purposely to provide the engineer with an opportunity to produce the best design instead of a less desirable performance design based on insufficient current. Test data show that the power requirements are about 150 mW from a 3-terminal, +9- and -9-V supply. The data also show that a 5-percent change in supply voltage yields approximately a 25- to 37-mV change in the amplifier zero setting. In actual use, it is anticipated that this supply voltage will change by less than 0.5 percent and, therefore, will cause a change in amplifier zero setting of 2 to 3 mV.

Temperature Range

The module must start and operate at any constant or variable (20° F/min maximum) temperature from -30° to +200° F. The module must not be damaged when subjected to a nonoperating storage of at least 6 hours at any temperature from -65° to +250° F.

Since the design consists of several integrated-circuit chips, storage temperatures are not a problem. In fact, the amplifier could be stored at any temperature from -65° to +300° F without damage. Because of the small size of the chips, which result in small temperature differences of critically matched components, a variable temperature does not appear to be a problem. Figures for the maximum spacecraft temperature gradient are not available now, but 20° F/min or less appears to be realistic. The heat-dissipation characteristic of the amplifier is satisfactory, and overheating does not occur within the operating temperature range. Performance of the amplifier within this range is discussed in the sections entitled "Output Bias and Offset" and "Gain Stability and Frequency Response."

Service Life

The module must be capable of operating for a minimum of 2000 hours, continuously or otherwise, during a service life of 1 year.

Since the amplifier design does not contain any moving parts or parts that will wear out, the life expectancy will be very long. It would be possibly as long as 100 000 hours. One amplifier has operated 5000 hours in a life test, and no change in characteristics has been evident.

Warmup Time

The module must be capable of operation with a warmup time not to exceed 50 μsec.

The amplifier design is such that the warmup time is well within specifications. Several units were tested by turning the power off and on with a mercury relay and observing the amplifier output signal referenced to the supply voltage on an oscilloscope. Figure 23 is a plot of the warmup characteristics of several amplifiers.

Input Signal

The module must be capable of receiving variable differential input signals from 0 to $\pm$5 V without damage.

In normal use, the maximum input signal will be about 7.1 mV for full-scale output. This specification was included to protect the amplifier from destruction by larger signals. The breakdown voltage of the input transistors is approximately 7 V. Therefore, a 5-V signal can be tolerated without destruction. If protection is desired for greater voltages, it can be obtained by adding protection diodes to the input circuit. However, diodes will introduce an additional source of error and reduce the performance characteristics. It is significant that a single-ended signal can be applied to the amplifier, but this will result in a shift in the amplifier zero setting. A correction can be made for amplifiers used in this mode.

Input Impedance

The input impedance must be 50 000 Ω or greater for any gain setting and for any frequency from dc to 5000 cps. A base current not exceeding 0.2 μA must be supplied internally to accommodate a floating source.

The input impedance to the amplifier proper is from 15 to 40 MΩ, depending, among other things, upon the gain setting and the temperature. However, a biasing circuit is required to accommodate a floating-signal source. With respect to the amplifier input terminals, this biasing circuit appears as two series-connected 50 000-Ω resistors that are in parallel with the input impedance to the amplifier proper. Since this impedance is large compared to the biasing impedance, the terminal amplifier input impedance becomes essentially the value of the biasing resistors, which is 100 000 Ω.

Output Bias and Offset

With a zero-input signal from a floating-source impedance of from 0 to 375 Ω, the module output must be capable of being set to 0 or 2.5 V. Selection must be by moving jumper wires between external leads. This output voltage must be within $\pm$50 mV of the ideal value over the environment range specified.

The difference in base currents of the two input transistors is the current that flows through the signal source. The base current of these transistors is 0.2 μA, but this may change by ±10 percent because of the manufacturing tolerances of the transistors. Therefore, worst-case conditions would result in a 0.04 μA current through the source. The voltage developed by this current through the source resistance appears as a differential signal to the amplifier input. For a fixed-source impedance, this error can be canceled out within the amplifier. However, a variable-source impedance will result in a shift in the amplifier zero setting. For example, assume a condition in which a source impedance would change from 0 to 1000 Ω. The worst-case shift in zero setting at a gain of 1000 would be 40 mV. This shift would be the majority of the error allowed by the specifications. Because of this, it was concluded that a specification requirement of a 0- to 375-Ω source (that could result in a 15-mV shift in the output) was a realistic requirement that could be accomplished. It has been determined in laboratory tests that the zero shift between 0 and 350 Ω is from 4 to 12 mV with an average of about 8 mV. The adjustments of the zero setting and the 2.5-V bias setting are satisfactory because these can be set easily to within 5 mV of the desired values. The temperature characteristic of the 2.5-V bias supply also appears to be satisfactory. The temperature characteristics of the zero setting, however, are not as satisfactory as desired. The test data, recorded in figure 24, indicate that from -30° to +200° F only 50 percent of the amplifiers are capable of being temperature-compensated to remain within the 1 percent allowed by the specifications. The remaining 50 percent may drift as much as 3 percent. All amplifiers could be compensated, however, to within 1 percent if the temperature range were reduced to the range of 0° to 160° F. An investigation of this problem has revealed that it is not serious for the reasons stated in the following paragraph.

The uncompensated amplifier has a nearly linear temperature coefficient. The bridge-arranged compensation circuit also appears to have a linear temperature coefficient. However, loading the bridge by the amplifier results in a nonlinear overall characteristic. The amount of this nonlinearity is a direct function of the current requirements of the uncompensated amplifier. This problem has been recognized and a solution formulated. Briefly, the solution is as follows.

Future fabrication will use transistors that are more closely matched and that have higher current gains. In addition, a new compensation circuit consisting of transistors and diodes will be developed to provide the required amount of linear temperature compensation.

Output Signal

The module must be capable of delivering output signals of from 0 to +5 V with the output bias set at either 0 or +2.5 V to a load of from 50 000 Ω to open circuit.

The amplifier design is such that this specification is met easily. In fact, output signals of greater than ±5 V can be amplified, as figure 25 indicates. In addition, the amplifier's output impedance is sufficiently low and has current capabilities to drive a load of 5000 Ω with loading effects of less than 1 percent.

Output Impedance

The output impedance of the module must not exceed 100 Ω from dc to 5000 cps.

The amplifier output impedance has been measured to be consistently less than 10 Ω, with the average centered around 5 Ω.

Voltage Gain

The voltage gain must be adjustable in steps within 1 percent of the ideal values of 700, 850, and 1000 V. This adjustment must consist of jumper wires connected between identified leads. No components may be added to change from one gain setting to another.

There is no problem in setting the gain to the 1-percent specification. In fact, most of the ranges can be set to better than 0.1 percent of the ideal value.

Gain Stability and Frequency Response

The gain of the module must be within ±1 percent of the dc value at 75° F from dc to 5000 cps. The frequency response must not change more than ±1 percent over the specified environment range.

As shown in figure 26, the frequency response of the amplifier is much greater than is required. It is desirable to reduce this response in future fabrication because the net effect will be to reduce the ripple on the output signal. There is no problem in modifying this response because the only change will be to increase the size of a capacitor. There is sufficient space within the amplifier to accommodate a larger capacitor. The gain stability of the amplifier did not meet the specification requirements. Typical variations were found to be from 1 to 2 percent. The variation is due to higher transistor-emitter, parasitic resistance than anticipated in the initial fabrication. The results are that typical open-loop gains are between 20 000 and 30 000 rather than the design value of 100 000. This can be corrected easily in future processing runs and is not considered a serious problem.

Output Ripple

The maximum output ripple voltage must be 25 mV peak to peak from dc through 15 Mc with a 90-percent confidence level measured over a period of 1 sec.

The amplifier design is such that this parameter is marginal. Typical amplifiers were measured to have an output ripple of 20 to 30 mV peak to peak. With the frequency response of the amplifier reduced as described above, this ripple will be reduced also. Therefore, this marginal design is not considered to be a problem.

Linearity

The module must have a linear output within ±12.5 mV of a straight line between the end points (nominal 0 and +5 V) with the output bias set at either 0 or +2.5 V.

The amplifiers exhibited a very good linearity curve, one that was well within the specification (fig. 27). With the higher open-loop gain as described for future fabrication, the linearity will be further improved.

Grounding Procedure

The signal input must be of the differential type and must accommodate a floating source. No external-input ground reference will be needed.

The amplifier design meets this specification. In addition, there are provisions through which a center-tapped source could be connected to the amplifier if the need ever occurs.

Common Mode

The module must have a common-mode rejection ratio of 80 dB or more for a 0- to 375-Ω floating-source resistance for frequencies from dc to 5000 cps and for voltages of ±1.0 V.

The design of the amplifier is satisfactory to meet the requirements of this specification, as indicated in figure 28. This characteristic will improve with a single-gain version because the common-mode rejection can be optimized for this gain rather than having a compromise for several gain settings.

Volume

The module must be 0.01 cu in. or less.

This specification was met by mounting the eight microminiature chips in a container 0.375 by 0.375 by 0.07 in., or 0.01 cu in. Actually, single-gain amplifiers mounted in containers 0.375 by 0.25 by 0.07 in., or 0.007 cu in., can be anticipated.

CONCLUSIONS

The development of a microminiature dc signal-conditioning amplifier has been completed with outstanding results, and the state of the art has been extended significantly. This development has proved that not only are signal-conditioning amplifiers of this nature feasible, but that with very little additional effort these amplifiers will be practical for use in space flight.

With no additional design effort, a limited number of flight-worthy amplifiers can be selected from a production lot. However, the test results indicate a need for improvement in the areas of open-loop gain, temperature-compensation circuits, and frequency response. Although improvements in these areas are considered to be minor, they would be advantageous because they would allow significantly increased manufacturing yield.

An analysis of the problem areas has determined the exact portions of the circuits in which corrective actions are required. A change in process techniques will lower the emitter parasitic resistance and result in an increase in open-loop gain. This increase in gain will improve the time and temperature stability characteristics to a high degree. A temperature-compensation circuit consisting of transistors, rather than resistance only, will improve the compensation characteristics. An increase in the value of the frequency-determining capacitor will reduce the amount of the output noise while maintaining the frequency response required by the specification.

Effort is being expended toward improving the dc amplifier in the form of ongoing work to incorporate the preceding suggestions. In addition, this effort will take into consideration the possibilities of simplifying the circuitry and extending the specification to include items such as output short-circuit protection and the capability of driving a load consisting of capacitance in addition to the required resistance.

Manned Spacecraft Center
National Aeronautics and Space Administration
Houston, Texas, May 24, 1967
904-02-13-09-72

TABLE I. - CHARACTERISTICS FOR FLAT-PACK INTEGRATED DIFFERENTIAL AMPLIFIERS

Vendor	Type	Input impedance minimum, MΩ	Input current maximum, μA	Input offset current maximum, μA	Input offset voltage at 25° C maximum, mV	Input voltage drift maximum, μV/°C	Common-mode rejection ratio minimum, dB	Open-loop voltage gain minimum (a)	Output impedance maximum, kΩ	Remarks
A	1	0.03		0.8	3	20	90	16	10	Specification from -55° to +125° C
	2	.5	0.4	.12	6	30	75	1.4	12	
B	1	0.01	10	2	5	10	70	1.4	0.5	
	2	.05	2.5	.6	7		60	.04	13	Room temperature specification
	3	.003	16	3	5		60	.1	.5	
C	1	0.02		2	5	4	90	0.4	6	Room temperature specification
	2	.1	.5		50	50	80	5	2	
D	1	0.1	0.6	0.04	1	10	65	4.5	0.2	Room temperature specification
	2	.2	.3	.02	1	10	85	4.5	.2	
E	1	0.1	0.8	0.2	10		83	1.2	0.90	
	2	.3			7		70	.04	13	Room temperature specification
	3	.15			2		80	.22	.5	
F	1	0.002	70	4	6			2.2		
	2		90	8	6			.1	0.12	Room temperature specification
	3	.08	2	.5	7		80	.05	11	
G	1	0.075	4	1.5	7			0.1		Room temperature specification
Requirement specification		2	1	0.1	0.02	0.5	90	100	0.1	Specification from -35° to +70° C

[a]All values are to be multiplied by 1000.

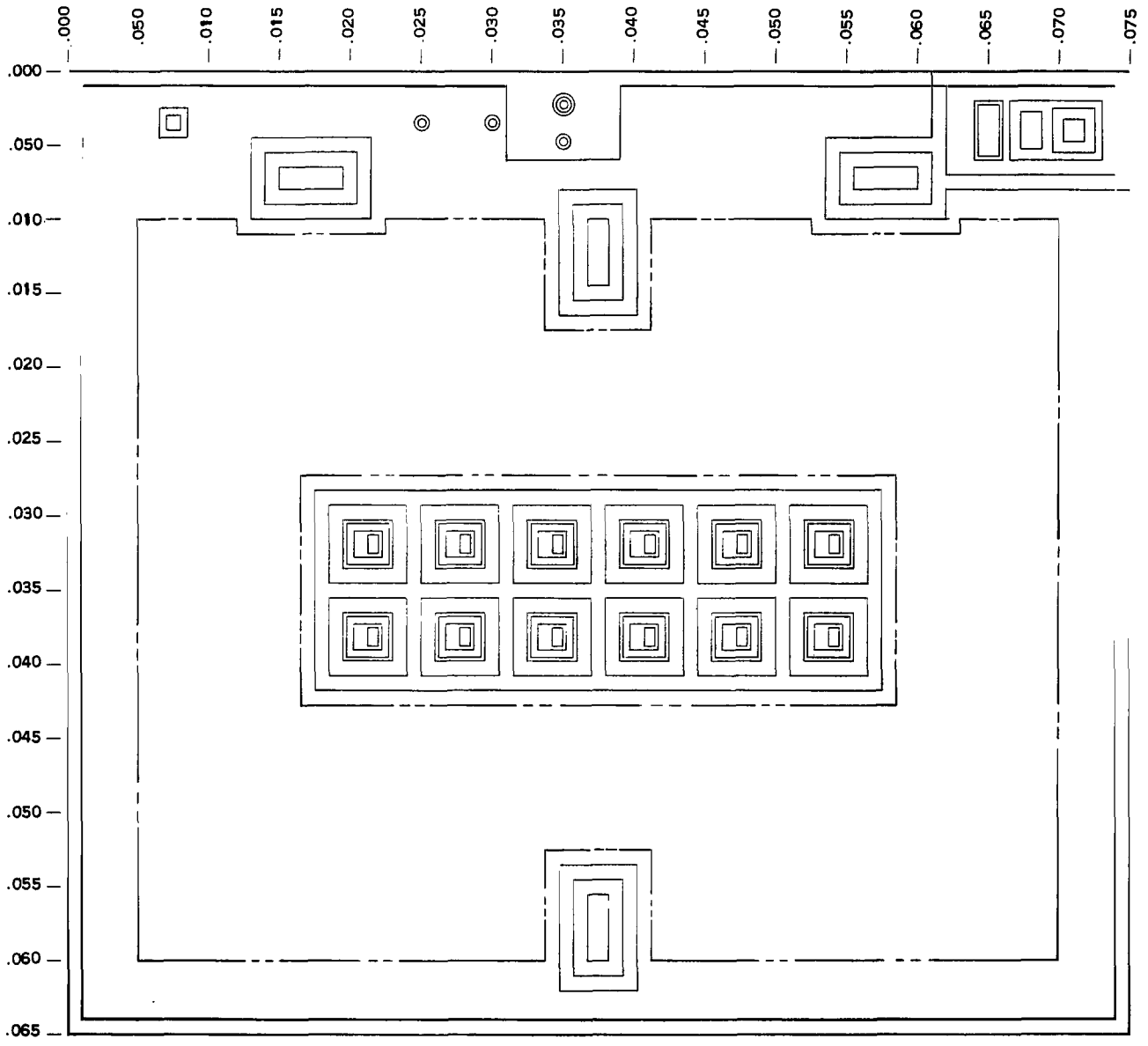


Figure 1. - Die, multicircuit subassembly.

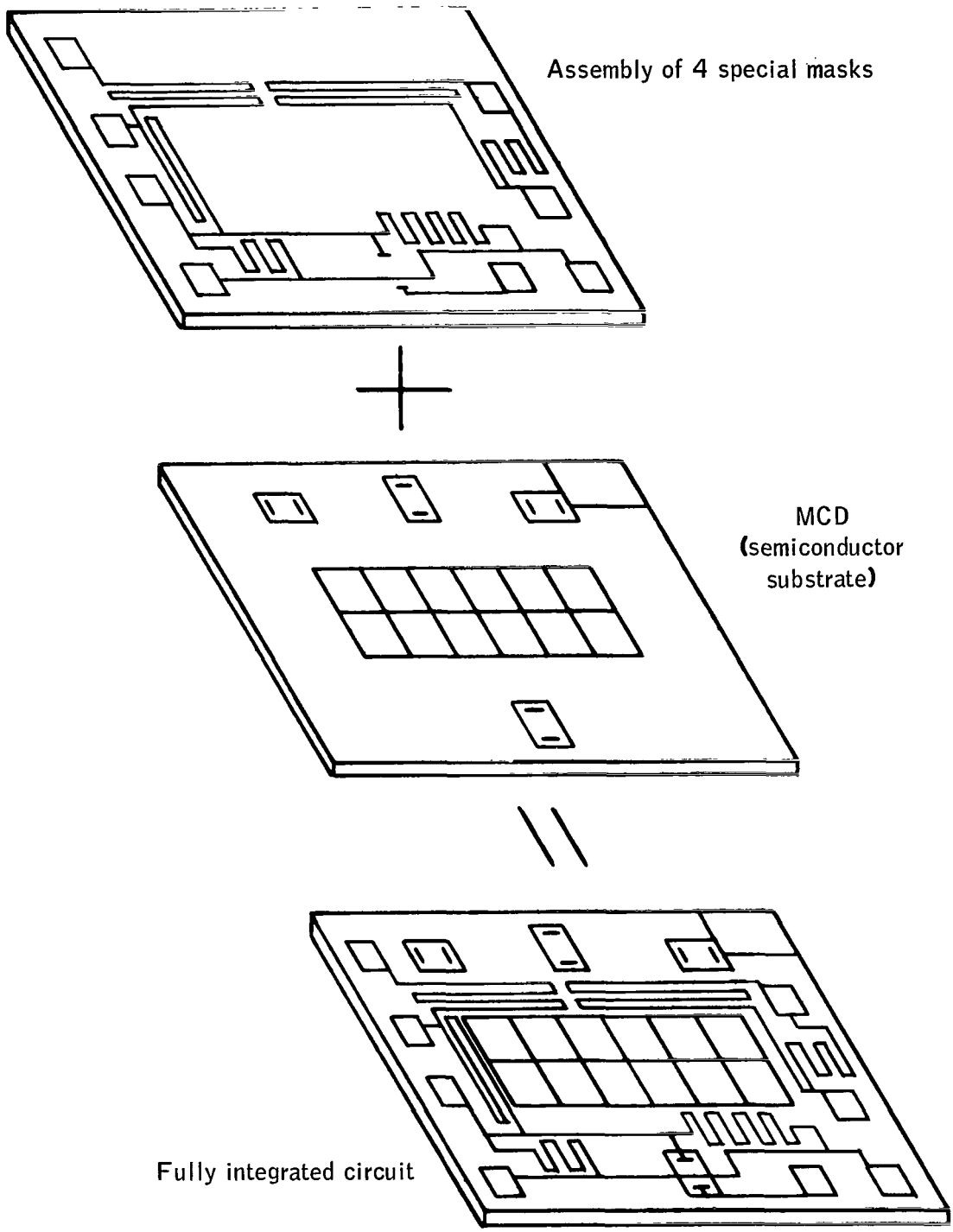


Figure 2. - MCD philosophy.

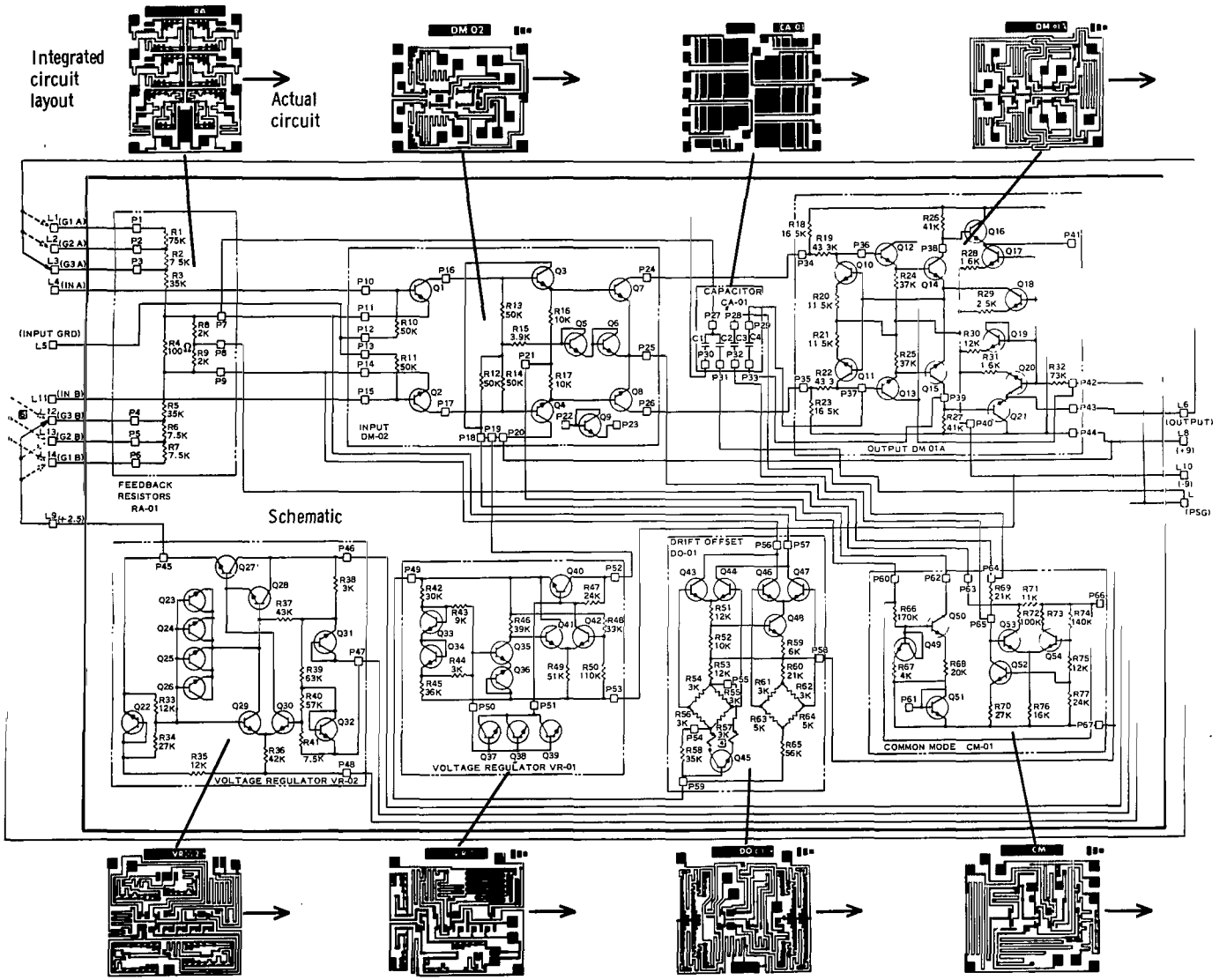


Figure 3. - Division of circuit into integrable sections.

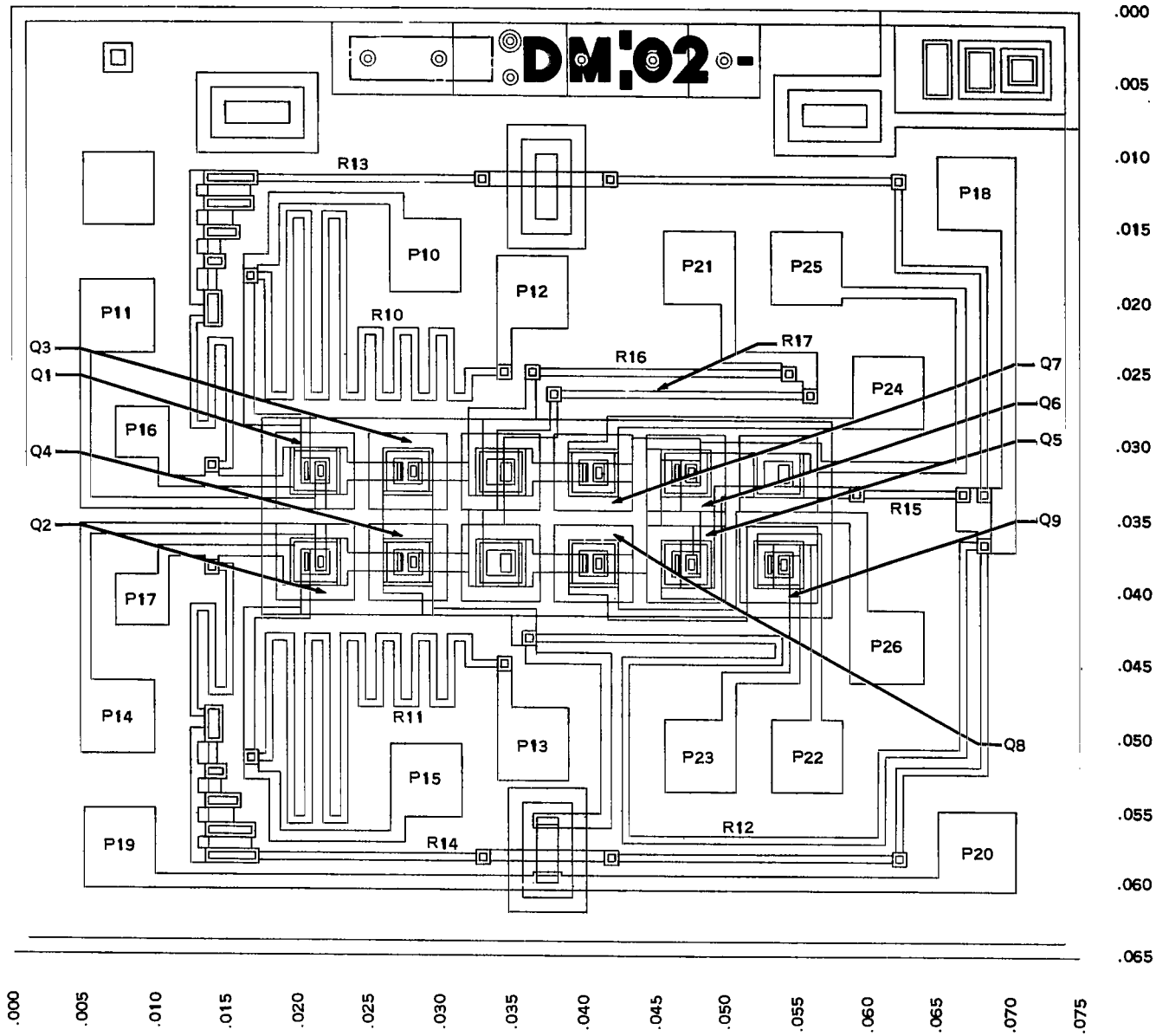


Figure 4. - Amplifier, direct-coupled, input chip.

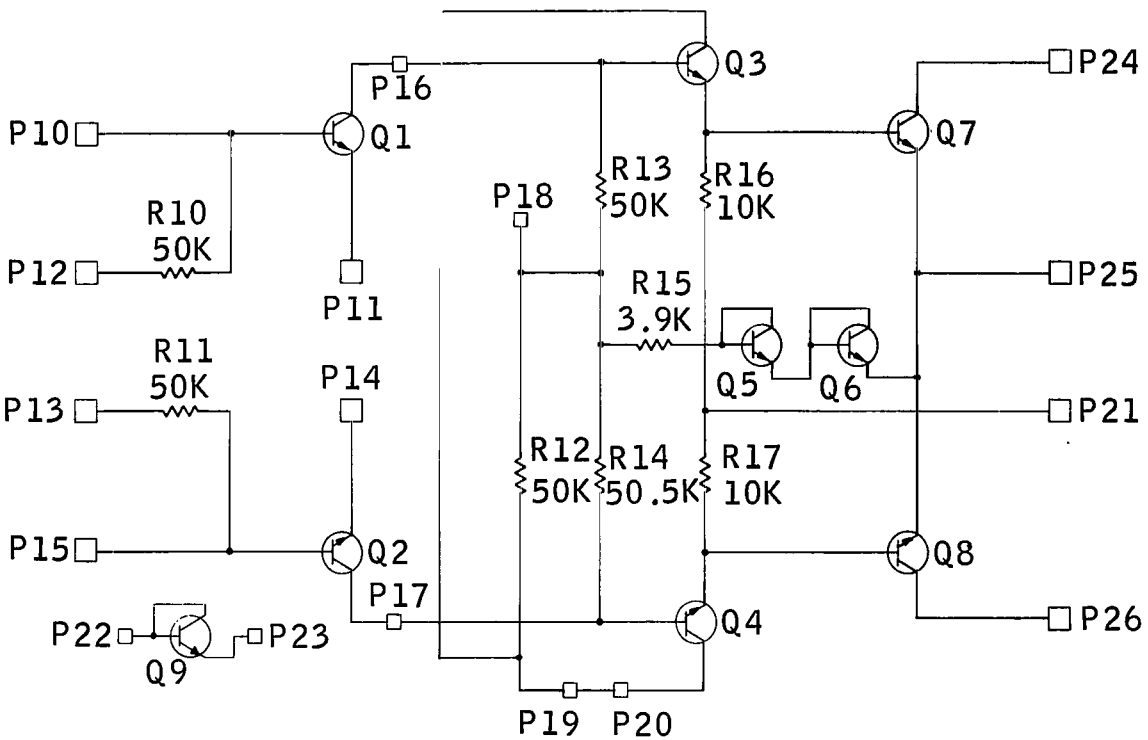


Figure 5. - DC amplifier input stage.

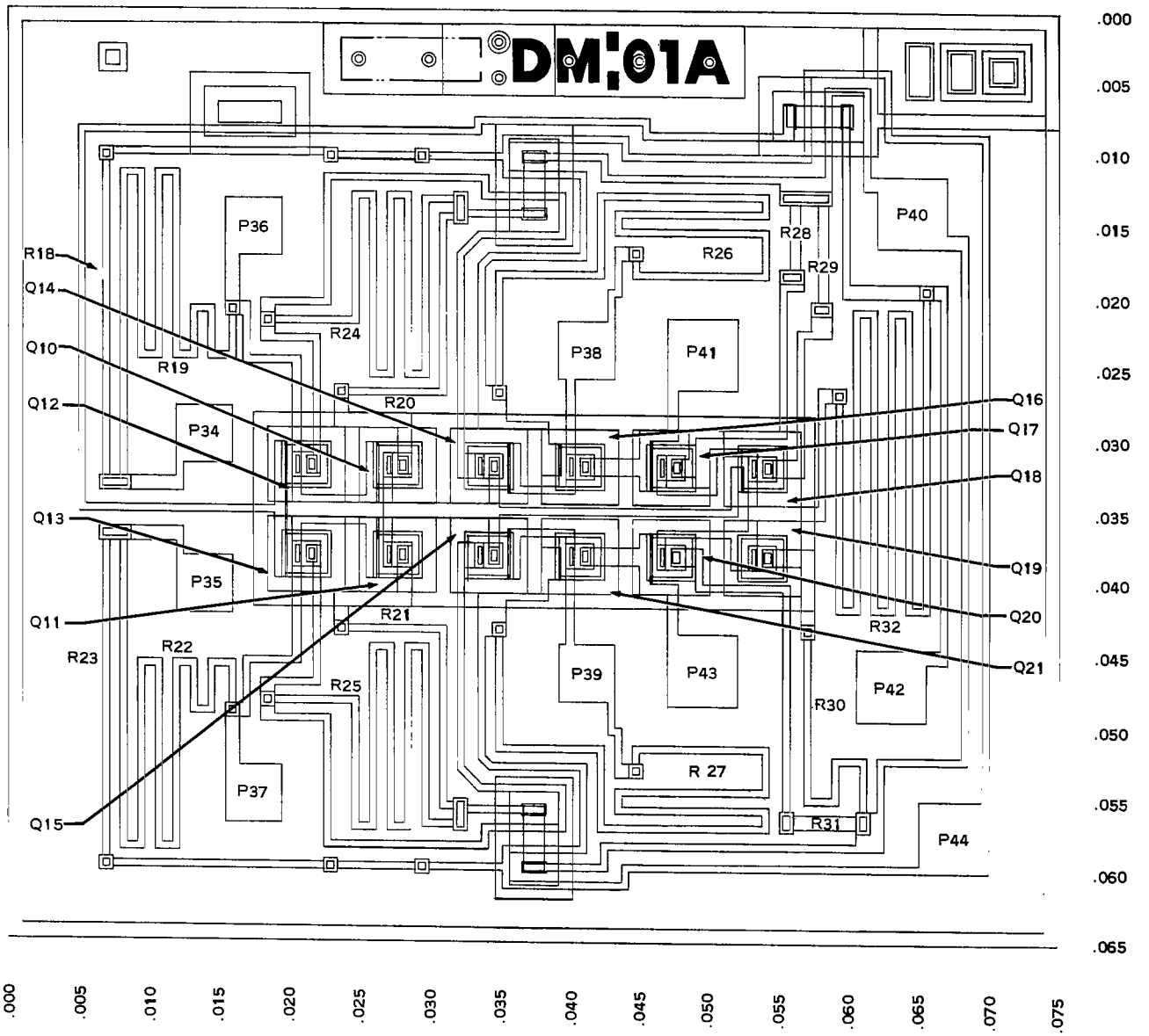


Figure 6. - Amplifier, direct-coupled, output stage.

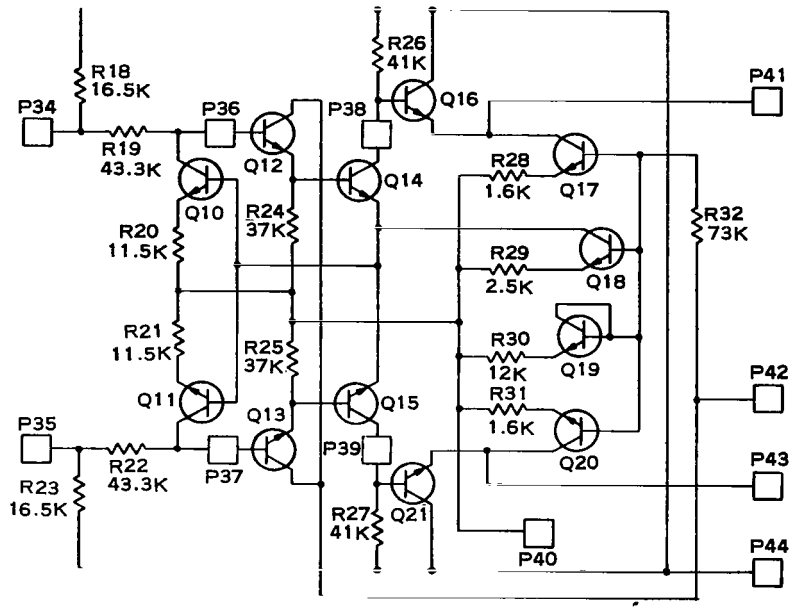


Figure 7. - Output stage.

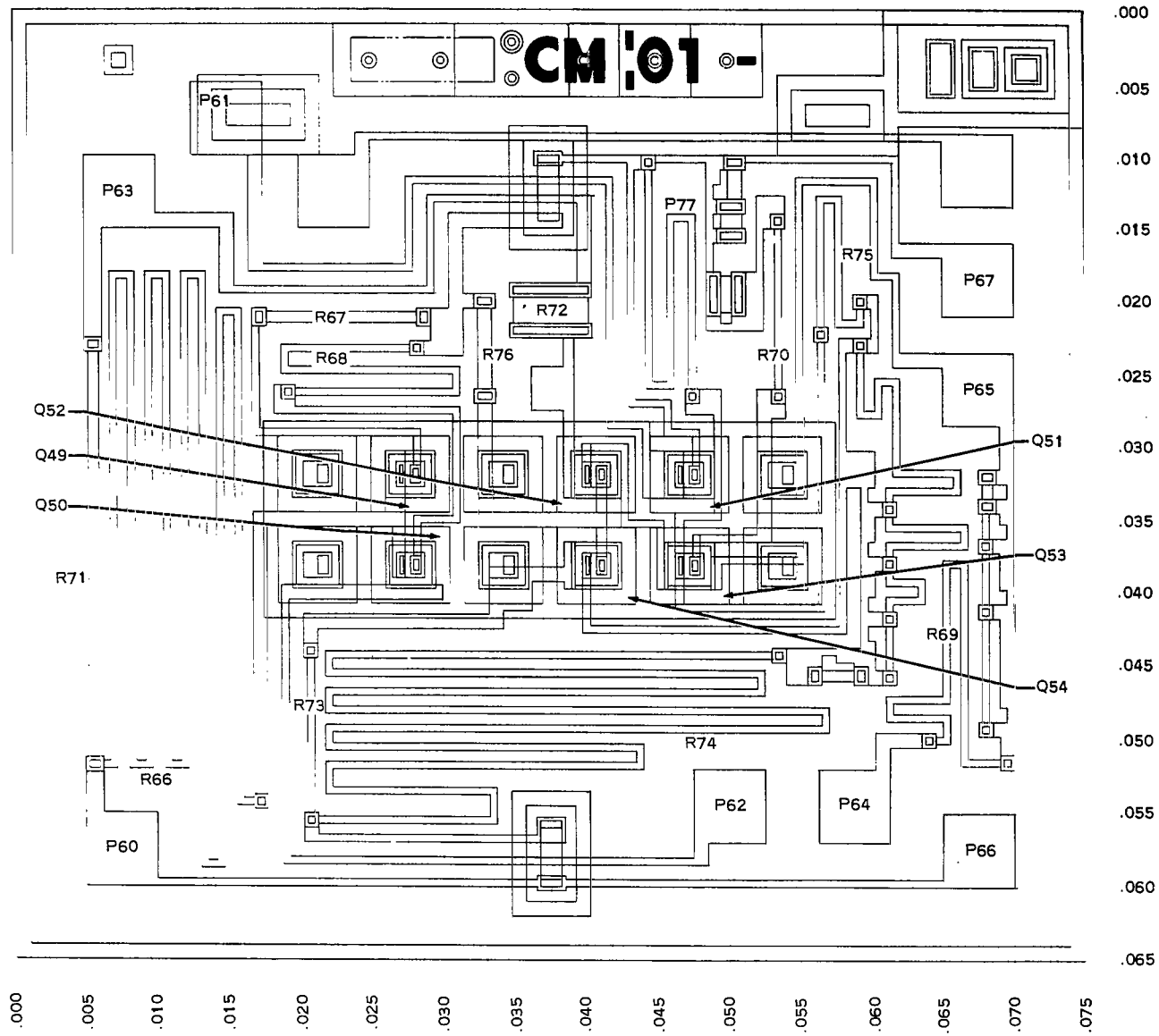


Figure 8. - Amplifier, direct-coupled, common-mode stage.

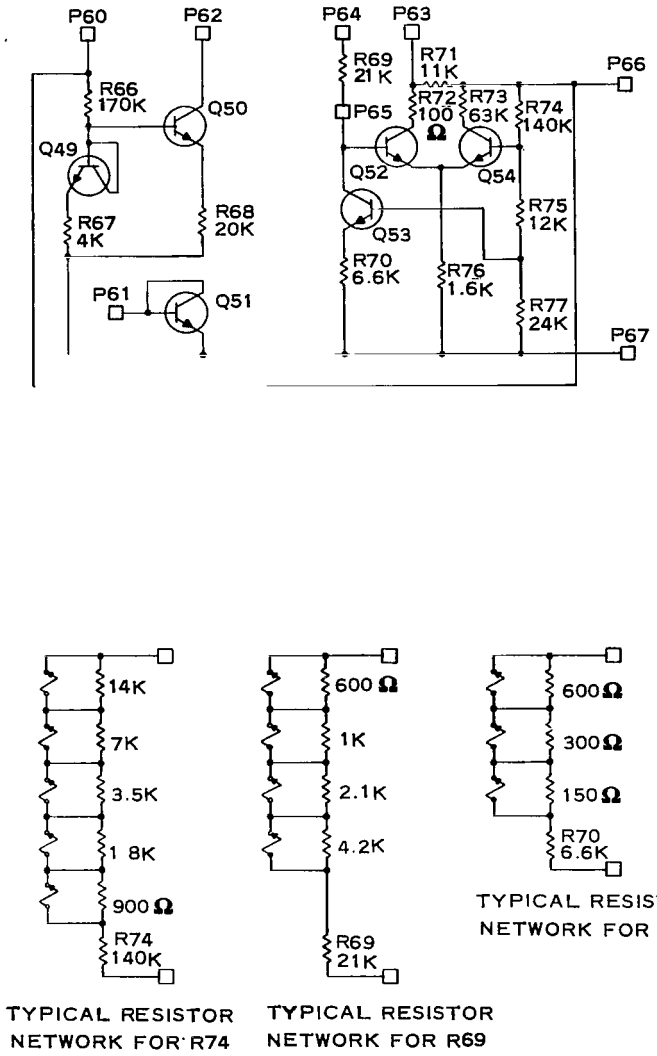


Figure 9. - Common mode.

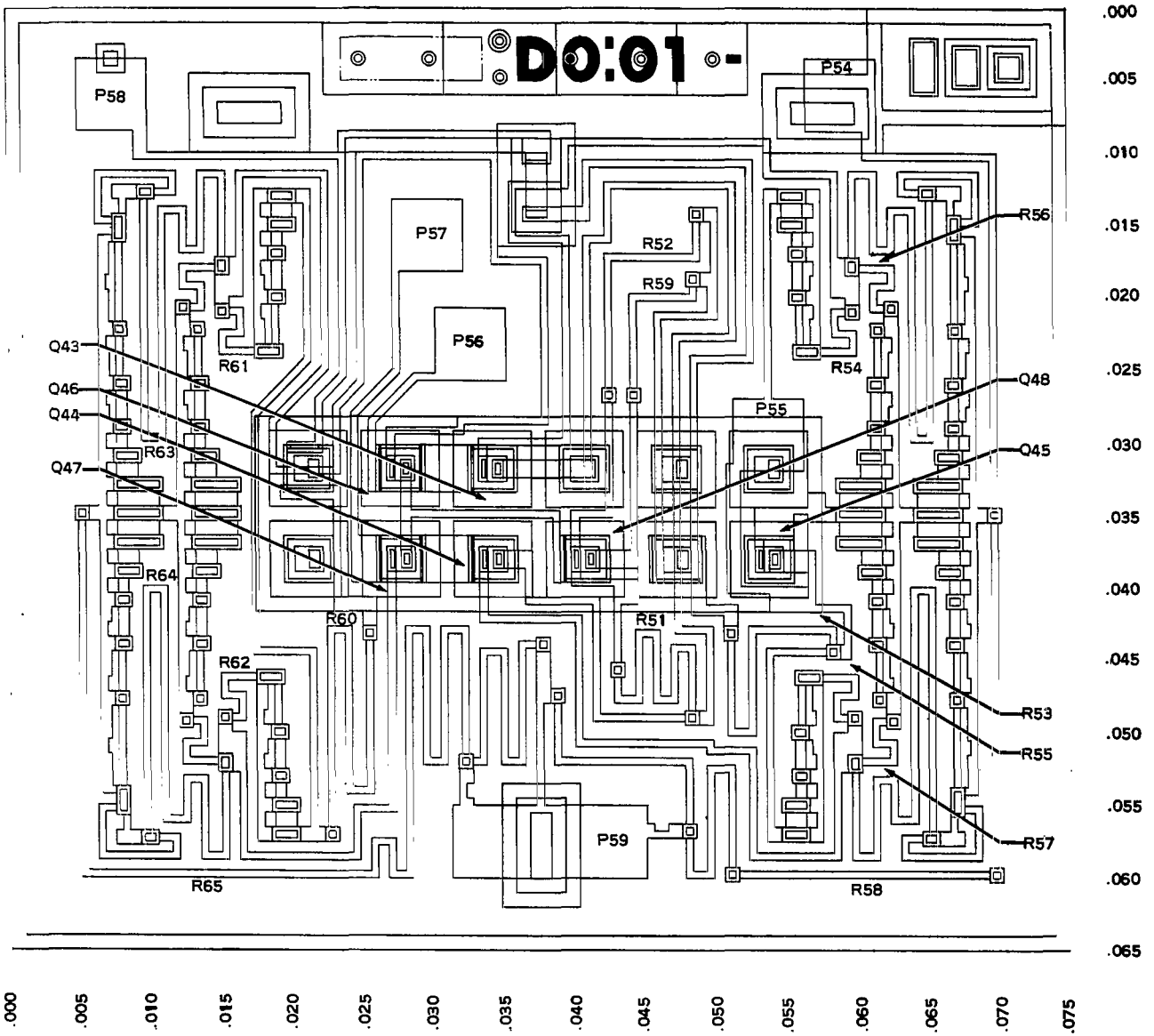
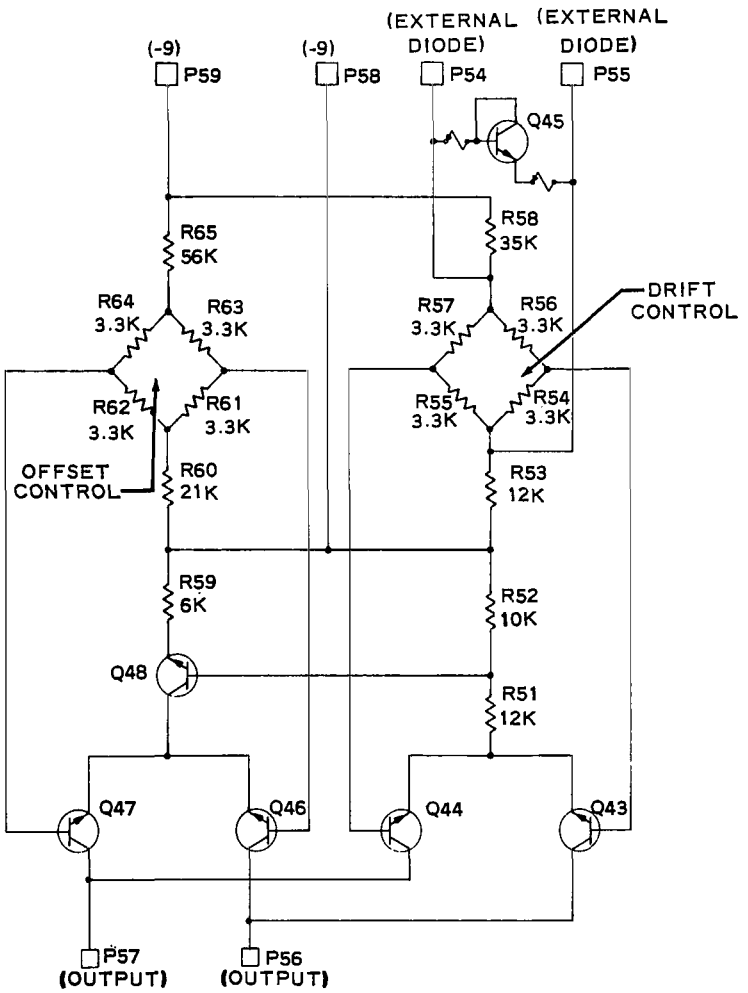
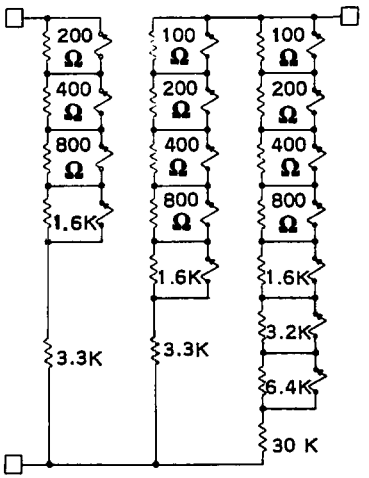


Figure 10. - Amplifier, direct-coupled, drift-offset stage.





TYPICAL RESISTOR NETWORK FOR R54, R55, R56, R57, R61, R62, R63 AND R64

Figure 11. - DC amplifier drift offset.

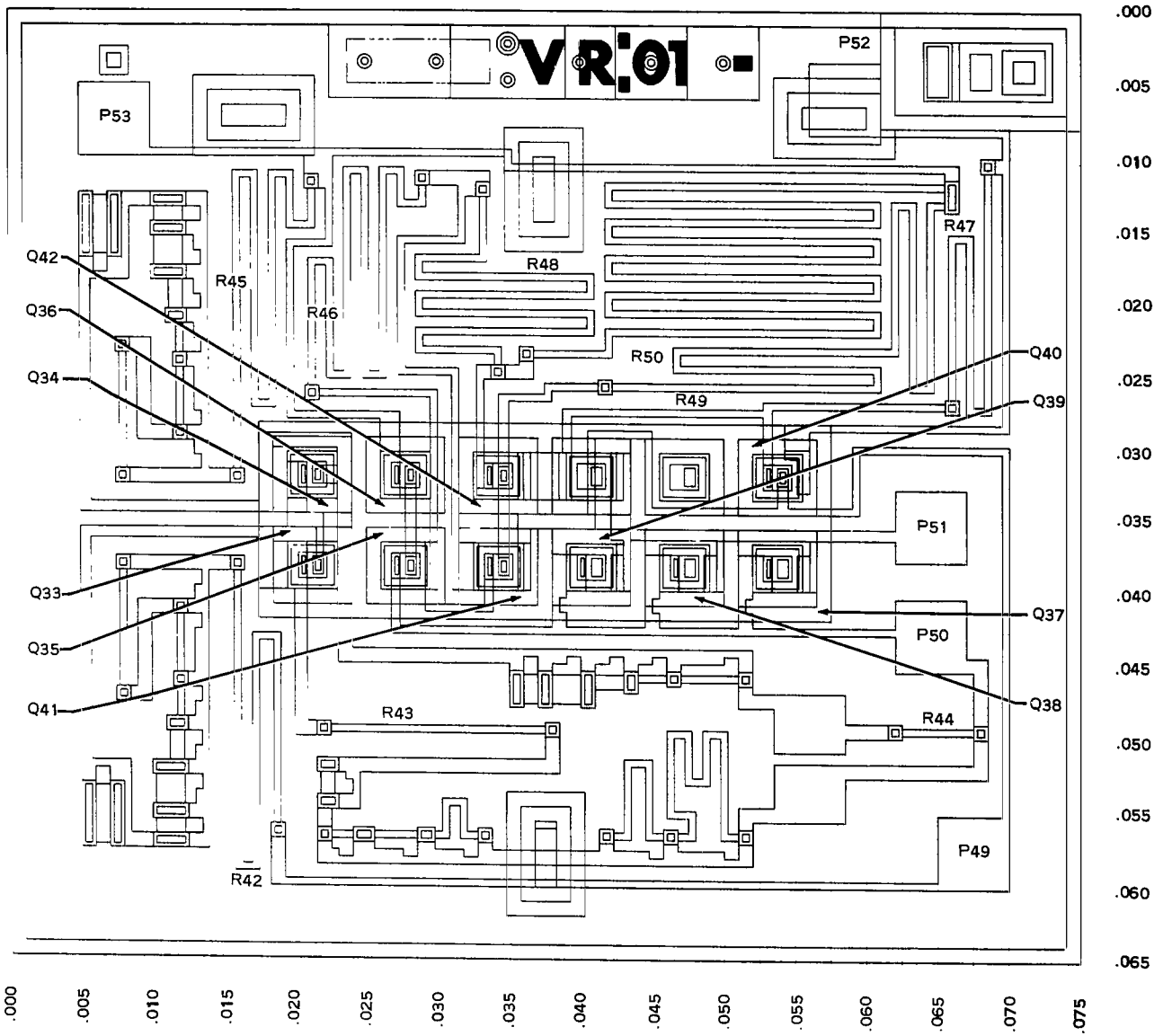


Figure 12. - Amplifier, direct-coupled, voltage regulator (VR-01).

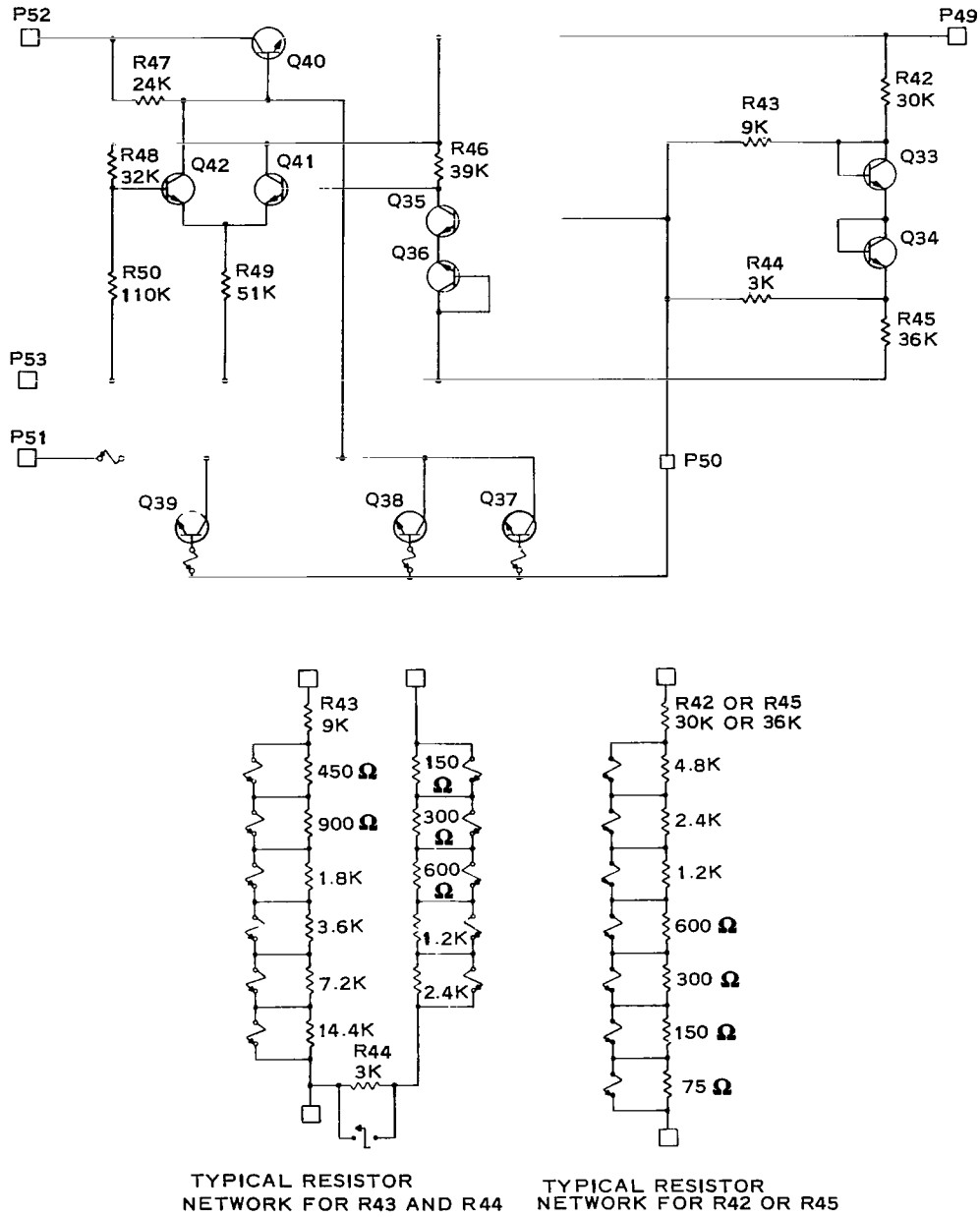


Figure 13. - Voltage regulator (VR-01).

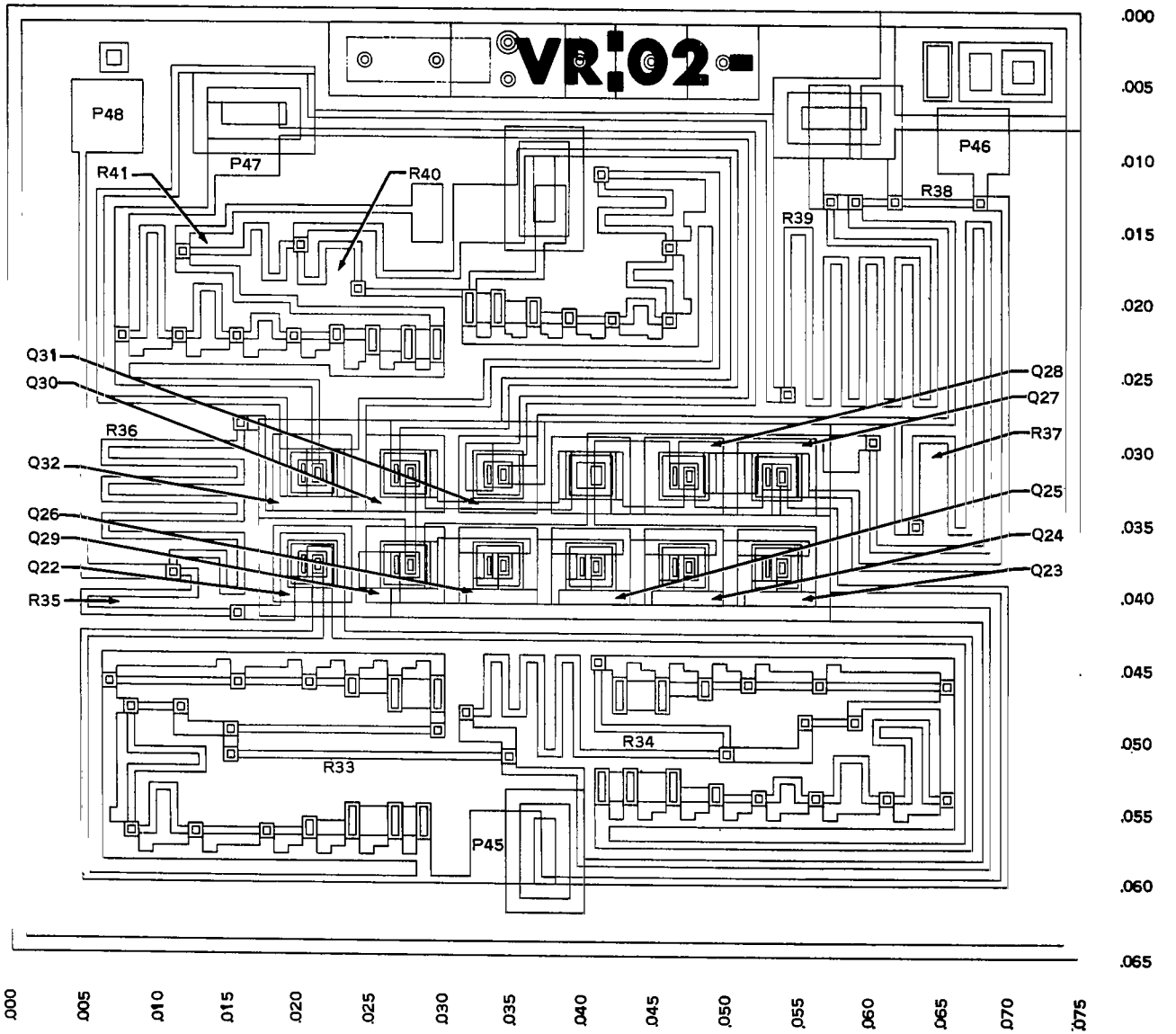


Figure 14. - Amplifier, direct-coupled, voltage regulator (VR-02).

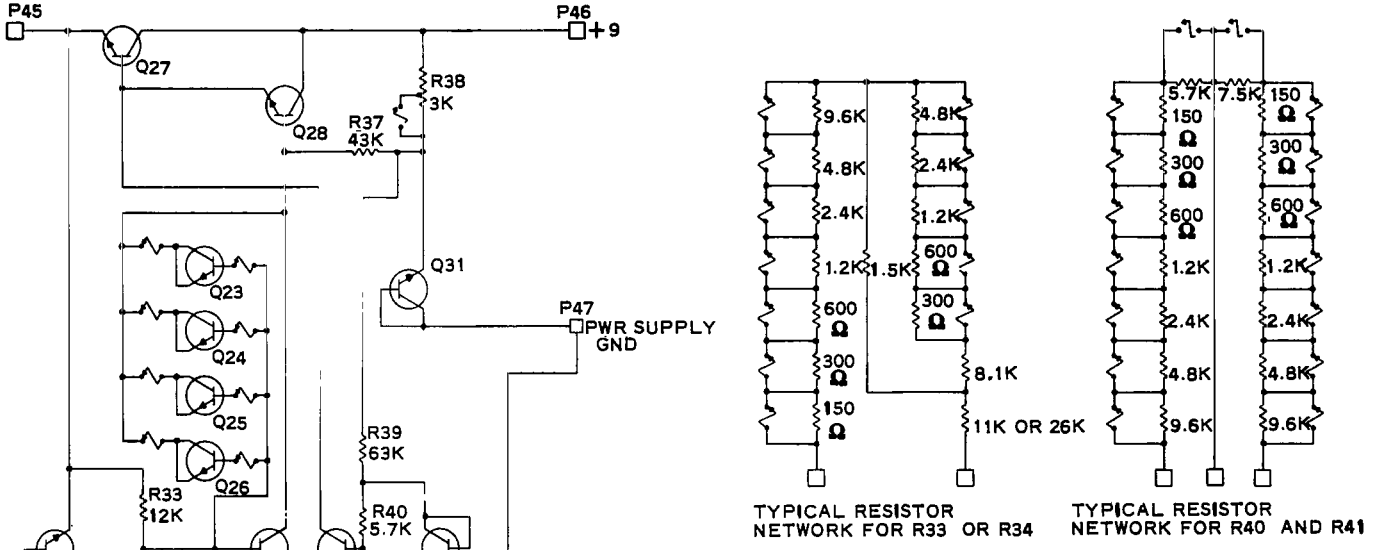


Figure 15. - Voltage regulator (VR-02).

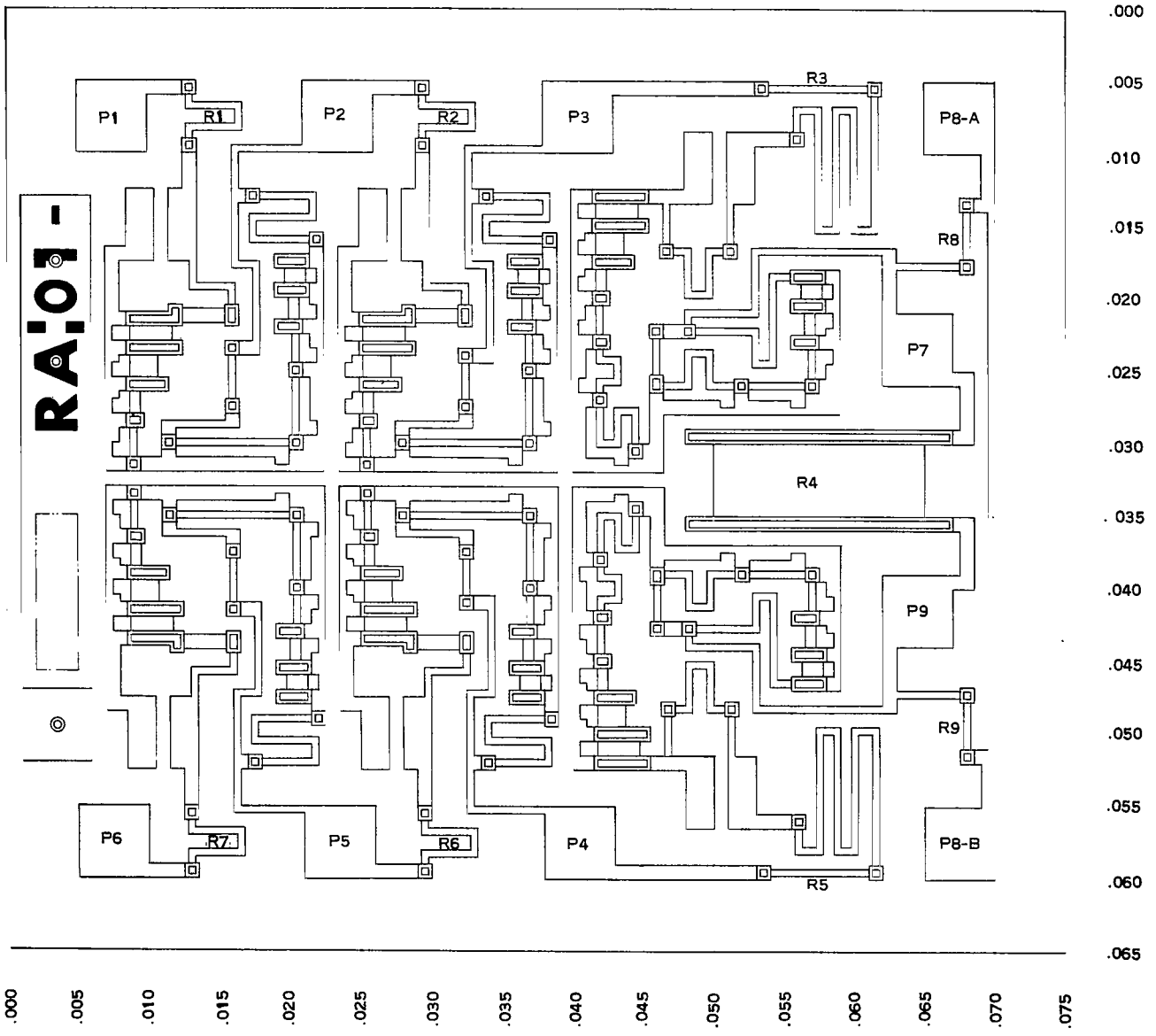


Figure 16. - Amplifier, direct-coupled, feedback resistor subassembly.

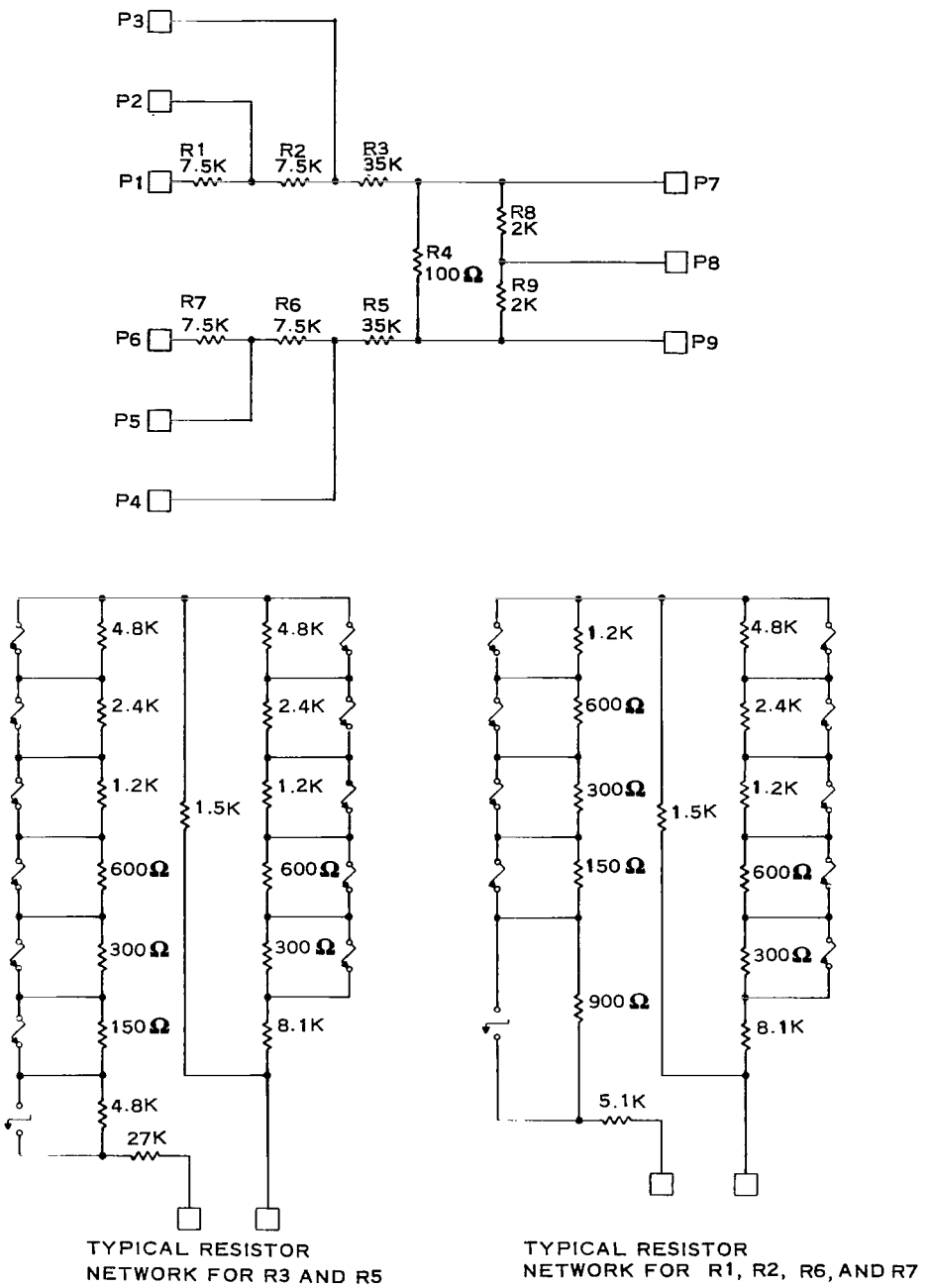


Figure 17. - Feedback resistor subassembly.

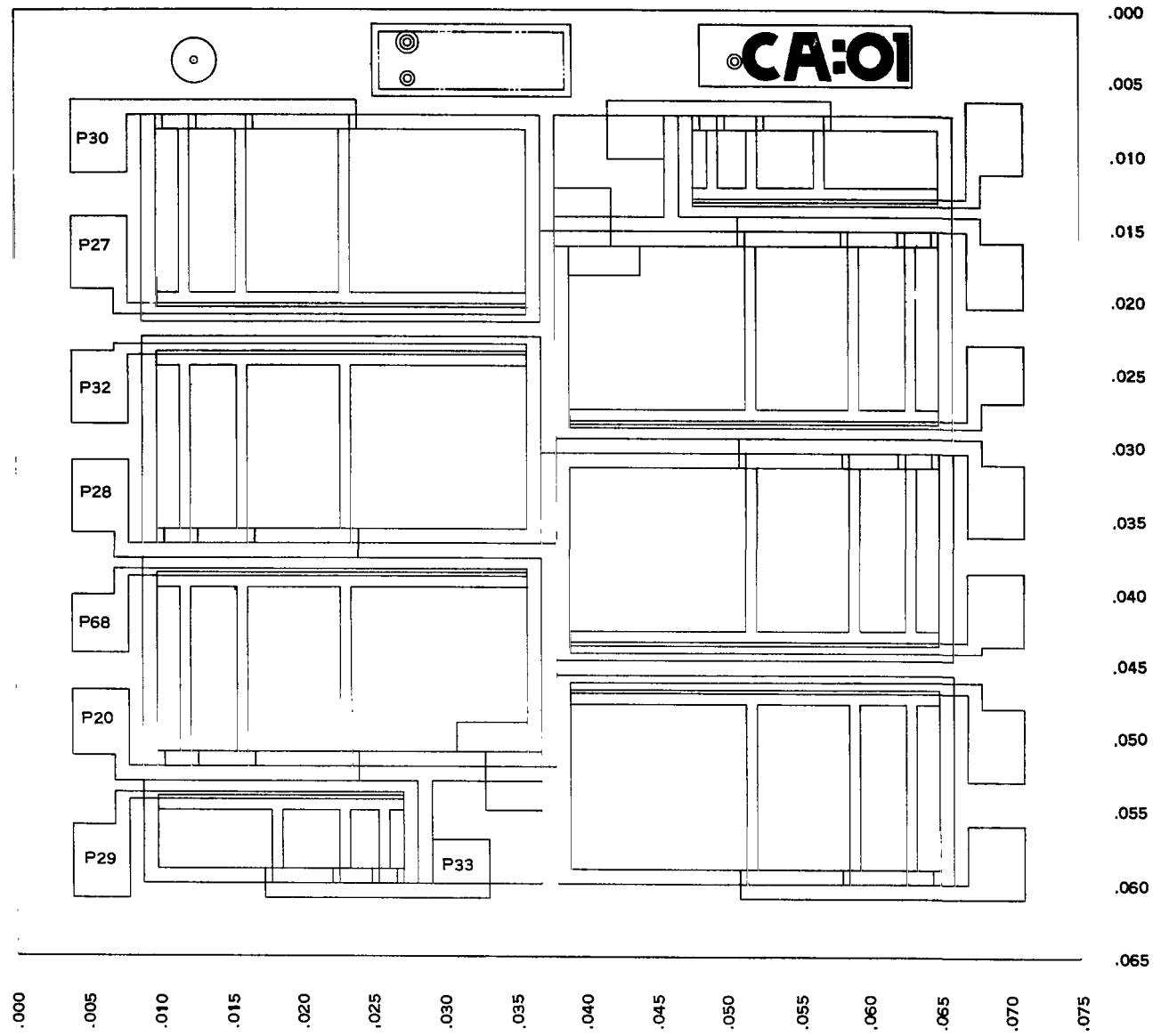
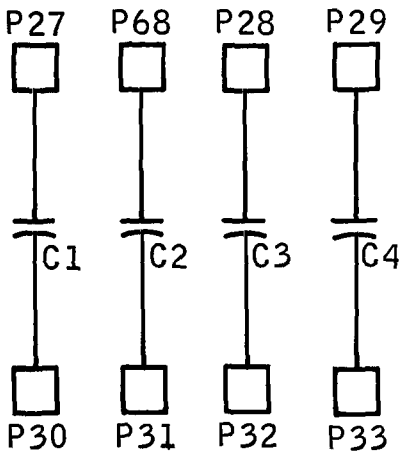
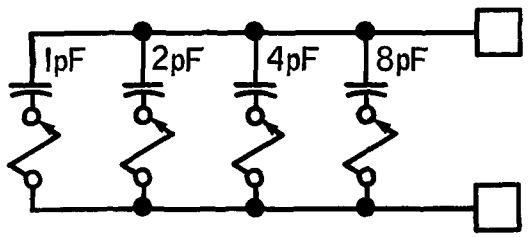
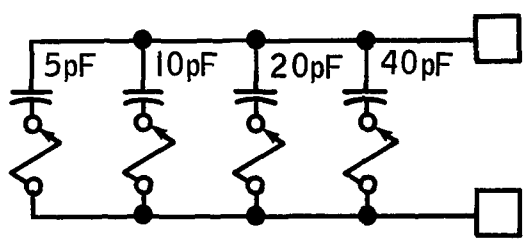


Figure 18. - Capacitor array.



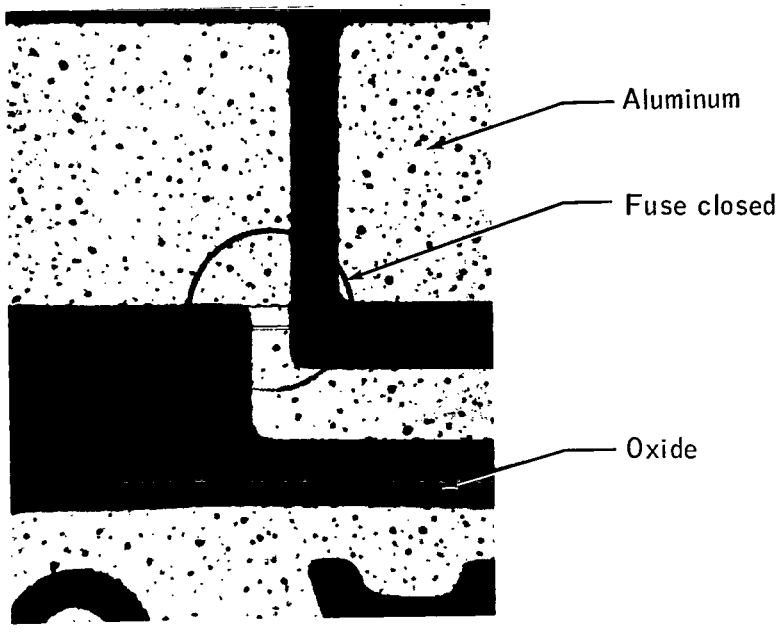


Typical capacitor network for C4

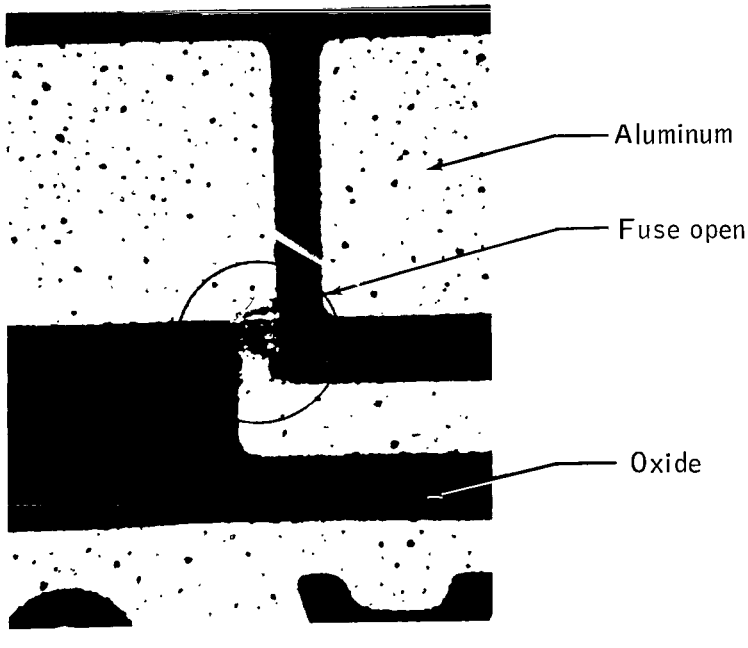


Typical capacitor network for C1, C2, and C3

Figure 19. - Capacitor networks.



(a) Before



(b) After

Figure 20. - Photograph showing how a fuse link is opened.

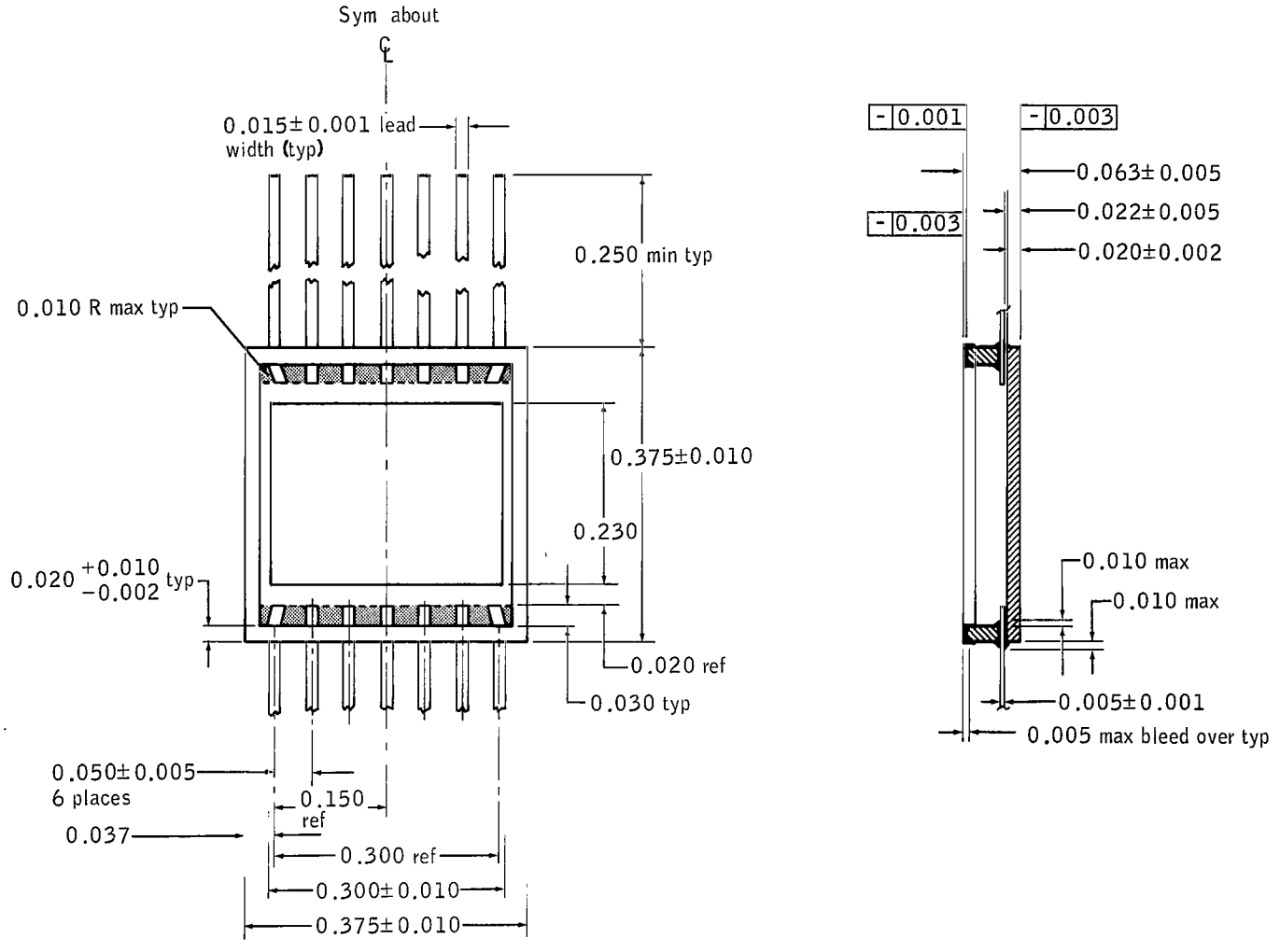


Figure 21. - Package drawing.

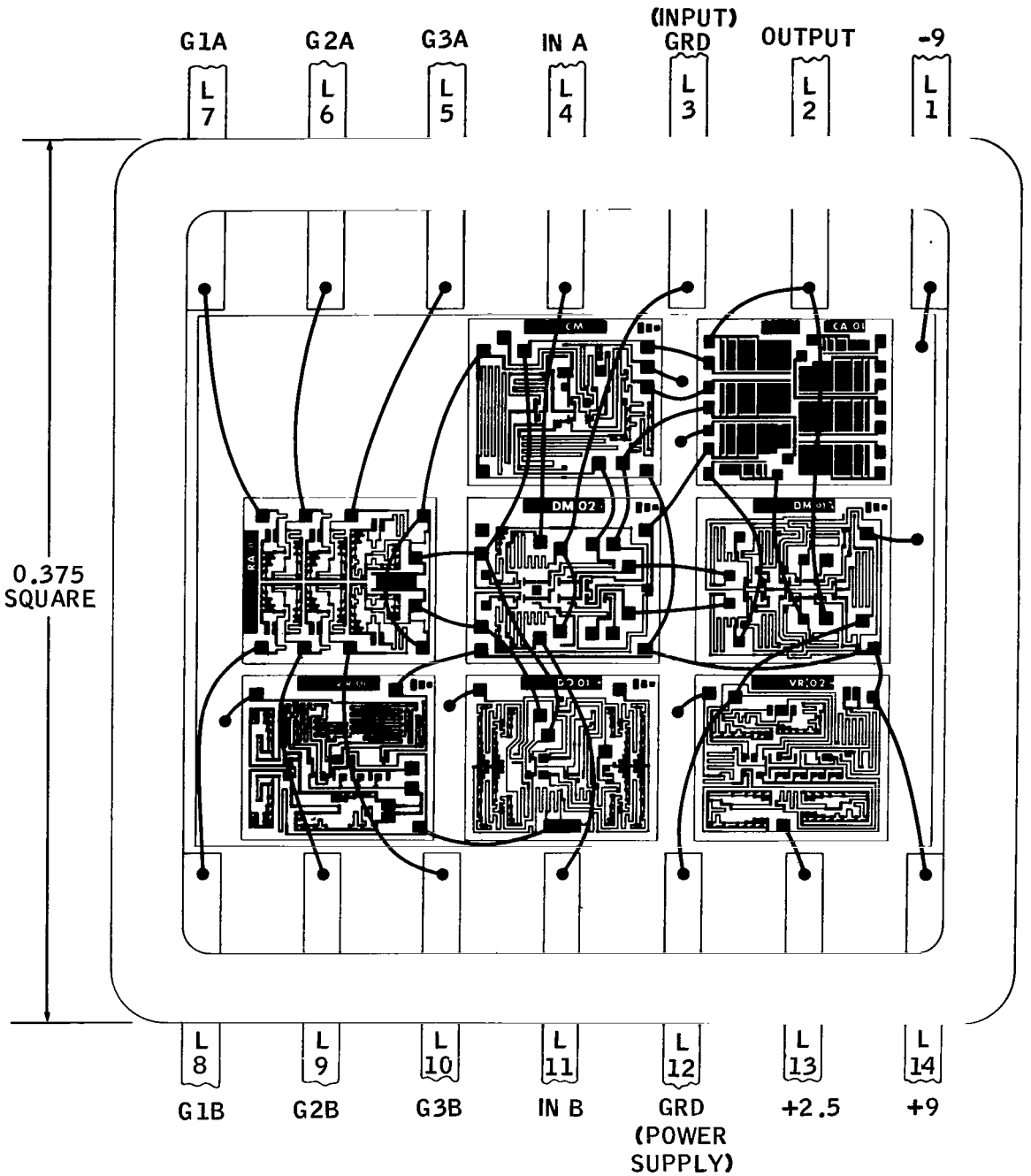


Figure 22. - Package layout drawing.

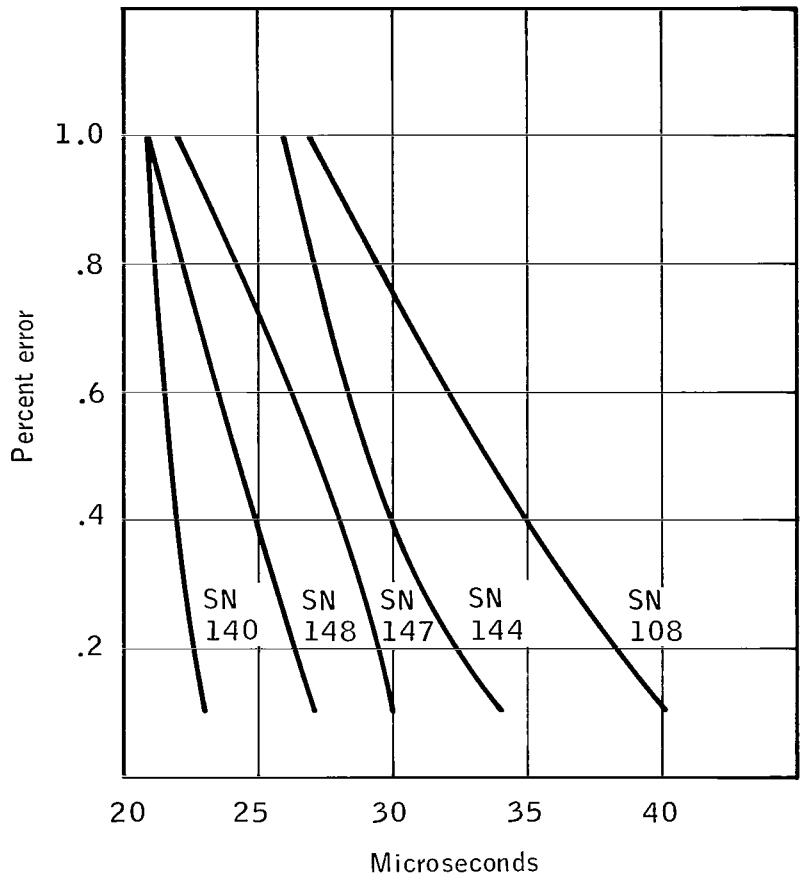


Figure 23. - Warmup time.

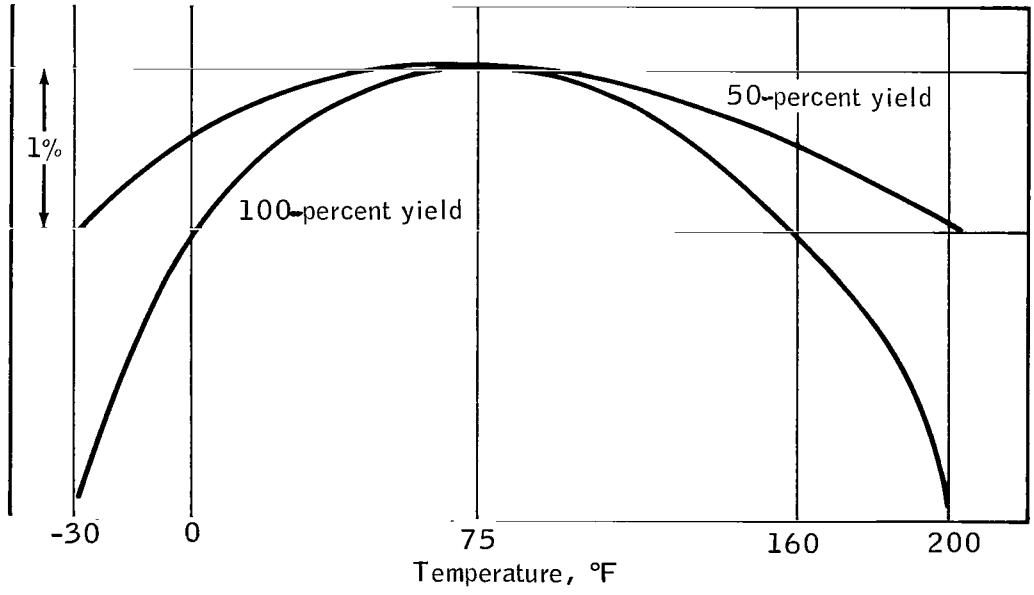


Figure 24. - Zero drift versus yield characteristics.

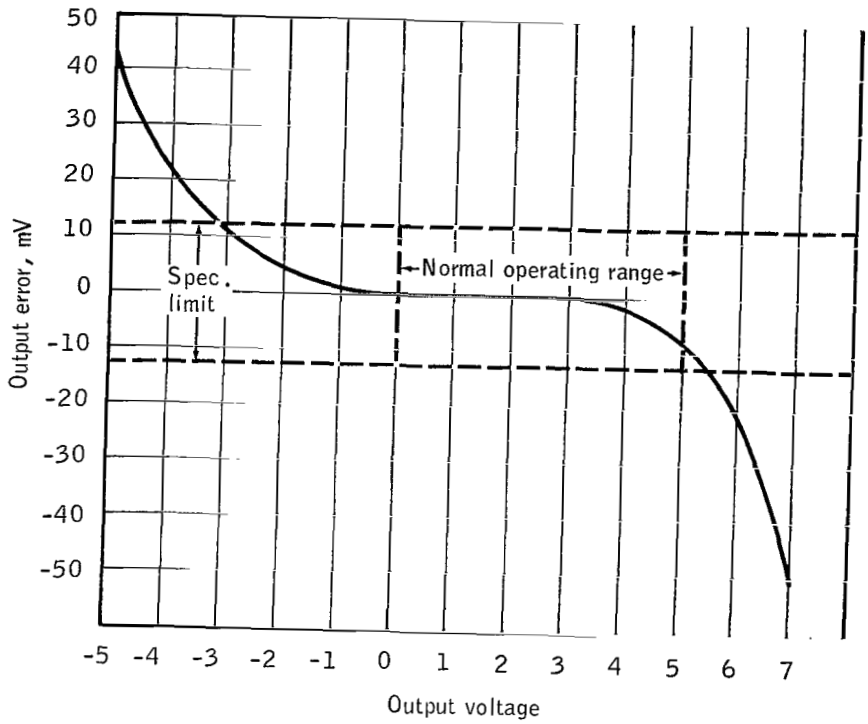


Figure 25. - Output capability.

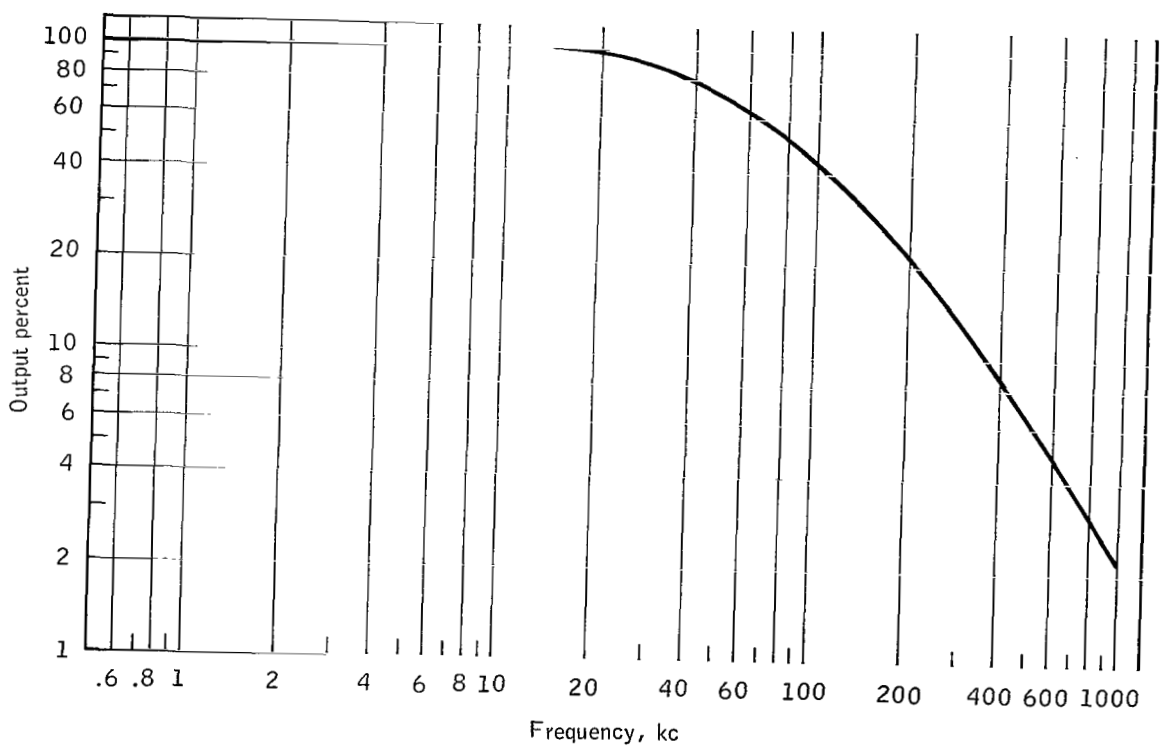


Figure 26. - Frequency response.

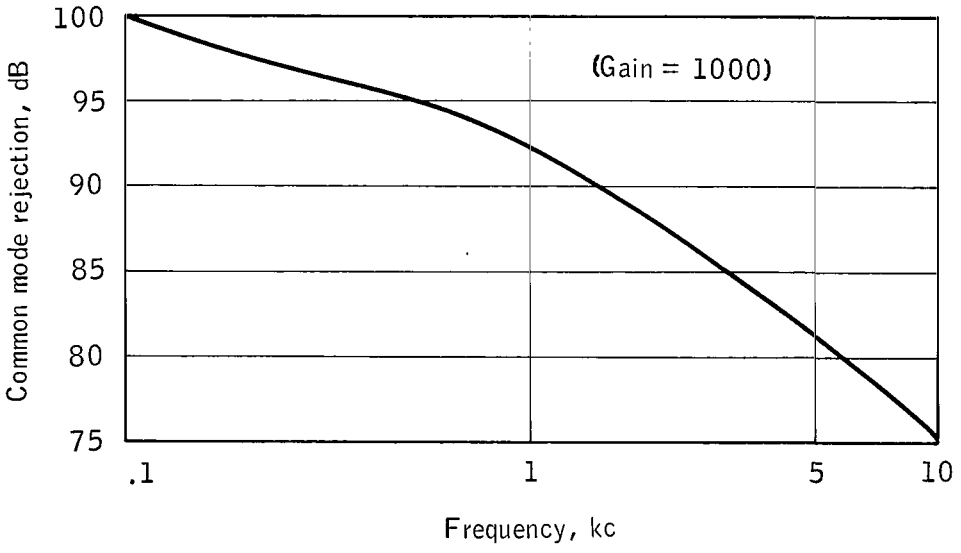


Figure 27. - Common-mode rejection.

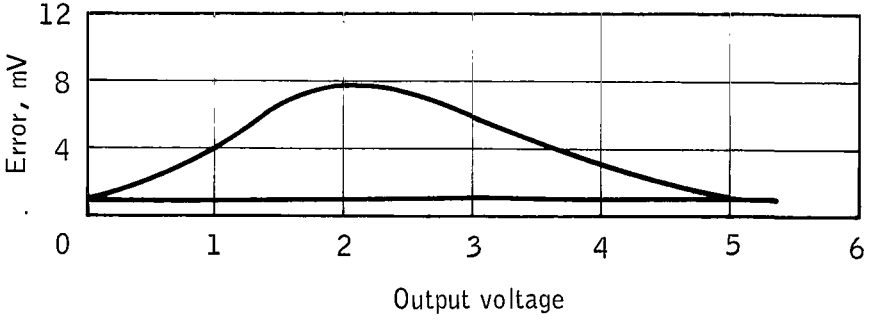


Figure 28. - Linearity.

APPENDIX A

AN INTEGRATED dc DIFFERENTIAL INSTRUMENTATION AMPLIFIER

By David Roy Breuer

This appendix indicates some of the present capabilities of the integrated circuit in the field of high-accuracy linear amplification. Low drift, high common-mode rejection, and high stable gain can be achieved now in the integrated-circuit form by applying the design principles described.

The close matching of transistor characteristics and the thermal intimacy of all portions of the compatible integrated circuit make it uniquely attractive for applications requiring high dc accuracy over a wide environmental range. The design of high-performance amplifiers, however, is complicated by the lack of potentiometers, transformers, inductors, and large capacitors. Also, ac and dc parasitics must be considered carefully to insure stable operation.

The following discussion will include the circuit design philosophy, component characteristics, and fabrication techniques needed to produce an amplifier with these specifications:

1. Direct-coupled differential input and single-ended output
2. Operating temperature -35° to +95° C (assumed for all specifications)
3. Selectable gains of 700, 850, and 1000 within 1 percent
4. Frequency response to insure 1 percent accuracy up to 5 kHz
5. Equivalent input drifts down to 0.2 μV/° C
6. Common-mode rejection $\geq$100 dB for dc to 5 kc
7. Selectable output offsets of 0 or +2.5 V, accurate to within ±50 mV
8. Input impedance $\geq$50 kΩ, dc to 5 kHz, for floating sources; >10 MΩ, dc to 5 kHz, for grounded sources
9. Output impedance <10 Ω, dc to 5 kHz
10. Output voltage swing of ±5 V into 25 kΩ load impedance
11. Floating source impedance of 360 to 0 Ω
12. Maximum quiescent input current into each input terminal of 200 nA

13. Power input of 100 mW

14. Power supply voltages may vary by ±5 percent

Feedback Techniques

Overall negative feedback from the output to the emitters of the input transistors, as shown in figure A-1, offers gain accuracy, low dc drift, minimum source-dependence, high input impedance, and low output impedance. Therefore, this emitter-type feedback is preferred for this application.

Switch S1, shown in figure A-1, is used to illustrate different modes of operation for the sake of discussion. In position 1, the amplifier is operating differential input and differential output. Assuming a perfectly balanced, symmetrical configuration, a differential-mode equivalent half circuit (ref. 1) can be drawn, as in figure A-2, to illustrate the differential-mode performance. The input stage is shown separate from the remaining portion of the amplifier. Analysis yields

$$\frac{v_o}{v_i} = \frac{R1 + R2}{R2}\left[\frac{1}{1 - \left(\frac{R1 + R2}{A_T R2} + \frac{R1}{A_T R_E}\right)}\right] \tag{A1}$$

where R_E = emitter diffusion resistance of input transistor, $A_T \simeq \left(\frac{R_L}{R_E}\right)A$, and A ≡ open-loop gain exclusive of the input gain stage. If A_T is very large, then

$$\frac{v_o}{v_i} = \frac{R1 + R2}{R2} \tag{A2}$$

which must always be greater than one.

The same gain equations apply to the case of switch S1 in positions 2 or 3 in which output B is effectively held at ground or E_R, respectively. The single-ended amplifier output A assumes the same potential as the reference for a zero differential input signal. This allows an offset to be applied to the amplifier output which is independent of gain setting.

The common-mode rejection for the single-ended and differential configurations are equal and dependent on the symmetry of the feedback impedances. For the particular design being considered, gain changes are mechanized by simultaneously selecting appropriate values for R1A and R1B. The gain is primarily determined by R1A, and R1B is correspondingly selected to give maximum common-mode rejection.

Since the common-mode rejection is particularly sensitive to the values of R1B, the +2.5-V reference supply required for this design must have a very low impedance to maintain maximum common-mode rejection for either output offset setting.

A block diagram of the overall base-type feedback connection which is used typically for operational amplifiers is shown in figure A-3. This configuration is unacceptable in this direct-coupled amplifier application because of the dc drift characteristics. To achieve closed-loop gains up to 1000, the feedback resistors must be very large. The nonlinear temperature-dependent input base currents and collector-base leakage currents of the input transistors must flow through these large resistances, creating excessive nonlinear temperature-drift components. In contrast with overall emitter-type feedback, the base and leakage currents of the input transistors flow only through the source impedance, allowing the nonlinear drift components to become negligibly small.

Also, in the case of overall base feedback, the closed-loop gain is directly dependent upon the source impedance in series with the feedback resistance R2. However, the closed-loop gain with emitter overall feedback is essentially independent of the source impedance. The closed-loop gain is affected by R_S (only as it affects the open-loop gain).

For emitter feedback, the closed-loop differential input impedance is found from feedback analysis (ref. 2) to be equal to the open-loop input impedance multiplied by the loop gain T, where T is the open-loop gain divided by the closed-loop gain. The closed-loop output impedance is equal to the open-loop output impedance divided by T.

Drift Considerations

With reference to the schematic diagram of figure A-4, direct compensation is accomplished by supplying a temperature-dependent current from the drift-offset control circuit to flow through the feedback resistor R4. This adds a linear temperature-dependent voltage in series with the input signal to cancel the accumulated inherent amplifier drift (ref. 3). The effectiveness of this drift compensation is directly related to the degree of linearity of the inherent and compensating drift components. Laboratory tests have shown equivalent input drifts less than 0.1 $\mu V/^\circ C$.

The predominant drift components of a differential amplifier are generated in the input stage and are primarily caused by circuit parameter unbalances. The perfectly balanced circuit would develop zero drift (and give infinite common-mode rejection). The main contributors to input-stage drift are differentials existing between the base-emitter voltages, current gains, and leakage currents of the input transistor pair. Each component is potentially nonlinear with temperature; however, with proper design techniques, they can be either linearized or minimized.

The differential collector-base leakage currents flowing through the source resistance develop the most nonlinear drift component, for it is proportional to the difference of two terms which increase exponentially with temperature. The silicon planar-diffused transistor of the present-day integrated circuit exhibits room temperature leakage currents of about 0.1 nA. Assuming a doubling with every 11° C rise in

temperature, this current increases to 0.1×2^7 nA at +100° C, which is less than 15 nA. For the 350-Ω floating-source configuration, the error at +100° C is

$$350\left[\left(0.1 + \Delta I_{CBO}\right) \times 2^7 - (0.1) \times 2^7\right] \text{nV}$$

where ΔI_{CBO} is the collector-base leakage-current difference (in nanoamperes) of the two input transistors at room temperature. This error is normally less than 2 to 3 μV and can be neglected. Note, however, that if overall base feedback were used, this drift term would have made the amplifier an impossibility.

Because of differential base currents, the most significant source-dependent drift term is caused by unequal transistor current gains which increase somewhat linearly with temperature. Assuming constant collector currents, the base currents decrease with increasing temperature. The voltage error is directly proportional to the source resistance and is minimized by the following:

1. Designing the input stage to operate at very low collector current levels
2. Maximizing the current gains of the input transistors
3. Maximizing the current gain match of the input transistors

Given the 200-nA input current specification, with minimum low-temperature current gains of 50, a maximum collector current is set at 10 μA. Since the source is floating, a +10-percent input transistor current gain match produces an equivalent input error of 14 μV at low temperature. The linear portion of this temperature error component can be canceled. If 5 to 1 compensation is assumed, an uncompensated error of 2.8 μV remains.

The base-emitter voltage is extremely temperature-sensitive, having a temperature coefficient of approximately -2.3 mV/° C. Assuming an identical pair of transistors, a 0.001° C difference will produce a 2-μV voltage differential. Low-level operation of the input stage enhances the drift performance at this point. For instance, if a transistor pair A is operating at a 10-μA collector current and at a 3-V collector-emitter voltage, a hypothetical thermal resistance of 500 °C/W leads to a 0.015° C temperature increase. In contrast, a transistor pair B operating at 100 μA and 5 V raises the temperature 0.25° C. The probability of maintaining exactly equal temperatures between transistors is much higher for pair A than for pair B. The thermal intimacy provided by the entire integrated circuit lends itself to minimum drift performance. A high degree of compensation results from insuring that the transistor input pair and the drift-offset control circuit experience the same temperature.

The differential base-emitter voltages of the input transistors is the dominant drift term. It can be shown that this component is highly linear with respect to temperature if the collector currents of the input transistor pair are held constant (ref. 4). It has been found also that maximum temperature tracking is obtained by selecting input transistors with the closest V_{BE} match (ref. 5).

It is the object of this design to hold the collector currents constant and equal. This results in a linear temperature-drift term which, together with the other accumulated drift terms, is compensated effectively by the drift-offset control circuit.

In figure A-4, the second stage is an emitter-follower pair. The equivalent input drift component contributed by the second-stage base currents is equal to this current differential multiplied by the emitter diffusion resistance of the input stage. If the second stage were not also operating at a very low emitter current level, namely 10 μA, this drift component could be quite significant. The emitter-follower second stage also provides a minimum dynamic load shunting the first-stage load resistor, thereby maximizing the first-stage gain. The collector currents of the input stage are held constant by a common-mode bootstrapping circuit, which will be described later.

Within the drift-offset control circuit, Q43 and Q44 form a differential amplifier which monitors a temperature-dependent bridge formed by Q45, R54, R56, and R57. The number of bridge unbalances determines the magnitude and direction of the drift-compensating currents in the collectors of Q43 and Q44. Likewise, Q46 and Q47 monitor the temperature-independent bridge formed by R61, R62, R63, and R64 to give offset control currents. The drift and offset currents are summed and fed to the 100-Ω feedback resistor to compensate for the accumulated inherent amplifier drift and offset components. Adjustments for zero drift and zero offset are mechanized by appropriately unbalancing the two bridges.

Common-Mode Rejection

The common-mode rejection factor (CMR) is defined as the ratio of the common-mode input voltage to the differential input voltage that gives rise to the same output voltage (ref. 1). Degradation of the CMR is caused by circuit unbalances. Three techniques are employed in this amplifier to insure high CMR:

1. Attention is given to obtain well-matched resistors.

2. Common-mode feedback is incorporated to decrease the effect of circuit unbalances by a factor equal to the common-mode loop gain and to increase the common-mode input impedance by the same factor.

3. Appropriate trimming of the overall feedback impedances maximizes the CMR. This adjustment tends to compensate for the effects of accumulated circuit unbalances.

One difficulty in using single-ended overall emitter feedback is the amplifier bias level dependence on common-mode input voltage and output voltage swing. For instance, considering the design values of this amplifier, the extreme conditions formed by a $\pm$1-V common-mode input and a 0- to +5-V output swing cause the currents in the feedback resistors to change more than 200 μA. Yet, the emitter currents of the input transistors must be stabilized at 10 μA. A high common-mode loop gain provides this stability and insures high ac CMR figures up through 5 kHz. This high-loop gain is obtained by incorporating two circuit features, a bootstrapping circuit and a common-mode voltage regulator amplifier.

The common-mode collector currents of the input transistors Q1 and Q2 are held constant by a bootstrapping circuit formed by R12 through R15 and by Q3 through Q8. The bias voltage across the load resistors R13 and R14 is forced to be equal to the voltage across R15. The diodes Q5 and Q6 maintain the voltage across the load resistors constant with temperature. The common-mode gain of this circuit is approximately R12/R15 $\simeq$ 12.5. Likewise, the effective common-mode load resistance is

$$1/2\ (R13 + R14)\ (R12/R15) \simeq 600\ k\Omega$$

The collector cutoff frequency formed by this effective load resistance and its associated capacitance is the dominant pole in the overall common-mode loop frequency characteristic.

Additional common-mode loop gain is obtained from the amplifiers Q52, Q53, and Q54. This circuit compares the emitter voltages of Q7/Q8 with a fixed reference and supplies the appropriate current to the emitter circuit of the input stage to keep the Q7/Q8 emitter voltage constant. This, in turn, stabilizes the operating currents of the input stage. Resistor R71 is needed to supply positive current as demanded by the feedback resistors. The lead capacitor across R69 is used for the purpose of high-frequency loop stability.

The total common-mode loop gain is approximately 46 dB. Consequently, the common-mode input impedance becomes

$$Z_{in(CM)} \simeq R71 \times \beta \times G_C > 100\ M\Omega$$

where β is the current gain of the input transistors and G_C is the common-mode loop gain. This impedance value is quite sufficient to maintain 120 dB CMR in the presence of a 5000-Ω unbalance in R10/R11 (assuming a 350-Ω floating source). Also, a 5-percent circuit unbalance within the common-mode loop becomes an effective 0.025-percent unbalance because of the 46-dB loop gain.

General Design Considerations

Three common-emitter gain stages develop a differential open-loop voltage gain of 106 dB, giving an effective single-ended loop gain of 100 dB.

$$A_T = \frac{(A_1)(A_2)(A_3)}{2} = \frac{(15)\ (55)\ (250)}{2} = 103\ 000$$

where A_T is the total open-loop gain, A_1 is the first-stage gain, and so on. The division by 2 results from the conversion to single-ended output. The specified temperature range gives rise to ±0.5-percent gain variations for a closed-loop gain of 1000. The first, second, and third gain stages operate at 10 μA, 100 μA, and 200 μA, respectively.

Special dc level shifting is needed because of the all-npn-transistor circuit configuration. This is accomplished by dropping the voltage across resistors R19 and R22. The currents are supplied by the current generators Q10 and Q11. The high dynamic impedance of the current generator minimizes signal attenuation. Emitter followers Q12/Q13 provide an impedance transformation into the third gain stage Q14/Q15. For the sake of biasing convenience, the base voltages of Q10 and Q11 are established by the common emitter voltage of Q14 and Q15.

The last gain stage is followed by an emitter follower Q21 to drive the currents demanded by the feedback and load resistors and also to lower the output impedance. It operates at 600-μA current, supplied by a transistor Q20 rather than by a resistor, to conserve power dissipation. The schematic and the actual integrated circuit are differential throughout. This feature is not needed for this particular application, since the unused side is left floating. Grounding is not necessary to meet the requirements of the single-ended overall emitter feedback previously discussed. Both sides are available, however, for applications requiring differential output signals. The three current generators, Q17, Q18, and Q20, have the bases tied together for convenience. The diode formed by Q19 is used for temperature stabilization of these current sources.

The loop-gain frequency characteristic of the differential portion of the amplifier includes four poles and one zero. The collector cutoff frequencies of each of the three gain stages represent three pole positions. The fourth pole is the dominant rolloff and is formed (approximately) by the accumulated capacitance at the base of Q13 and the resistance R22. This dominant pole is controlled with a capacitor C4, connected from the base of Q13 to the collector of Q15. It is multiplied because of the Miller effect. The loop-gain zero is created by the capacitor C1 in shunt with the feedback resistor. This corner appears as a zero in the loop-gain response and as a pole in the closed-loop-gain response.

Voltage regulator VR-01 supplies regulated power to the drift-offset control circuit to increase the power supply rejection of the entire amplifier. Isolation from power supply variations is required because of the nature of the drift-offset control circuit. In review, drift and offset are compensated by intentionally unbalancing the two resistor bridges. However, this simultaneously sensitizes the circuit-to-power supply variations. The integrated voltage regulator allows this power supply dependence to be diminished to about 1 μV equivalent input error because of a 1-percent power supply voltage change.

Transistor Q40 is the series-regulating transistor controlled by the differential amplifier formed by Q41 and Q42. Transistor Q36, connected as a diode, is reverse-biased to breakdown and is used as the primary reference. Transistor Q35 samples the output and compares it with the 7-V zener reference. Transistors Q33 and Q34 are forward-biased and used for temperature drift compensation. Resistors R43/R44 and R42/R45 can be trimmed to give zero drift and zero offset, respectively. Transistors Q37, Q38, and Q39 are used as rolloff capacitors for high-frequency

stabilization. A common transistor structure is used successfully as transistor, forward-biased diode, zener reference diode, and capacitor.

Voltage regulator VR-02 provides a precise +2.5-V reference potential with the following specifications: output voltage, +2.5 V ±0.1 percent with respect to ground; temperature stability, output ±0.1 percent over -35° to +95° C range; line regulation, $<\pm 0.1$ percent output stability for ±10 percent line variations through 100 kHz; output impedance, $<1\ \Omega$; and operating current, 0 to 5 MA.

In this circuit, Q27 and Q28 are the series-regulating elements controlled by the Q29/Q30 differential amplifier. The zener reference is Q22, and Q32 is forward-biased to give temperature-drift compensation. A zener used to increase the regulation against positive input voltage changes is shown as Q31. Transistors Q23 through Q26 are used as rolloff capacitors. Adjustment of R40/R41 controls drift primarily, while R33/R34 controls offset. These resistors can be adjusted to give the desired characteristics.

Integration

The complete amplifier, including regulators, contains 135 components. Present fabrication yield necessitates dividing the circuit into separate integrable sections. The following eight modules were chosen on the basis of circuit function and equal complexity (fig. A-4):

Module type	Components
Input	Transistors and thin film resistors
Output	
Common mode	
Drift-offset control	
Drift-offset voltage regulator	
Offset reference regulator	
Feedback resistors	Thin film resistors on silicon
Capacitors	Dielectric isolation metal on silicon capacitor

The first six modules are fabricated on a common-active substrate (MCD) containing 12 transistors and 4 diffused crossunders. These MCD are converted to a unique circuit by depositing appropriate resistors and aluminum interconnections. This approach allows stockpiling of wafers before circuit commitments are made, thereby significantly decreasing fabrication lead time and fabrication costs.

The minimum-geometry, buried-layer, epitaxial transistors (the smallest dimension is 0.25 mil) provide excellent high-frequency performance and maintain high current gains at very low current levels. Some pertinent characteristics are as follows:

Characteristic	Typical value
dc current gain	
I_c = 1 mA, V_{CE} = 2 V	150
I_c = 10 μA, V_{CE} = 2 V	75
High-frequency current gain	
f = 100 MHz, I_c = 3 mA	8.5
I_c = 1 mA	6.5
I_c = 100 μA	2.0
I_c = 10 μA	0.4
Collector-base capacitance	
V_{CB} = -2 V	1.4 pF
Collector-substrate capacitance	
V_{CS} = -10 V	2.2 pF

The resistors are evaporated cermet thin-film structures with the following characteristics:

Width	0.5 mil
Absolute tolerance	±20 percent
Ratio tolerance	±1 percent
Absolute temperature coefficient	200 ppm/°C
Ratio tracking temperature coefficient	10 ppm/°C

Adjustment is accomplished by evaporating metal shorting links (by passing high current via probes) to increase a resistor value in binary related increments. The smallest actual resistance step is 150 Ω; however, within an appropriate resistor network, this value is made to appear as low as an effective 5-Ω step.

The capacitor module is fabricated with a new dielectric isolation technique whereby collector-substrate isolation is provided by an oxide insulation layer. This removes the dc leakages normally associated with the typical pn junction isolation. It also decreases the parasitic substrate capacitance to about 15 percent of the capacitor value. A thin layer of oxide is grown over an area of heavily doped N+ silicon. Aluminum is evaporated over the thin oxide. One capacitor plate is the aluminum and the other is the N+ silicon. Two sizes of capacitors are available on each module: a 75-pF type, adjustable in 5-pF steps; and a 15-pF type, adjustable in 1-pF steps. Each module contains a total of 480 pF.

The package layout is shown in figure A-5. Gain selection is made by connecting the output to G1A, G2A, or G3A, and simultaneously making the corresponding ground connection to G1B, G2B, or G3B. A +2.5-V output offset is selected by replacing this ground connection with the +2.5-V connection. The package size is approximately 0.375 in. by 0.375 in. outside dimensions.

The integrated instrumentation amplifier described in this appendix yields drift characteristics which are competitive with high-performance chopper stabilized amplifiers. In addition, the gain, gain accuracy, and common-mode rejection characteristics make this amplifier an exceptionally useful microminiature building block for real-system applications.

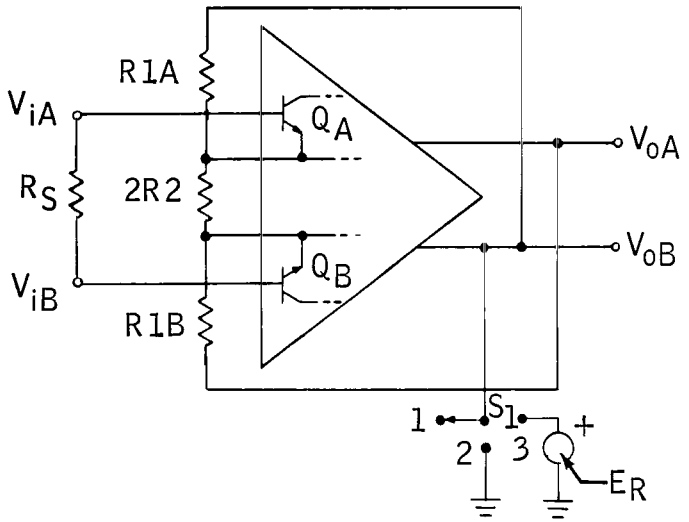


Figure A-1. - Overall emitter feedback.

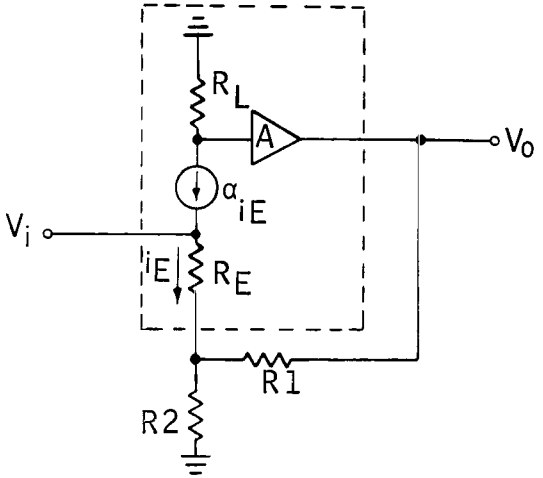


Figure A-2. - Differential equivalent circuit.

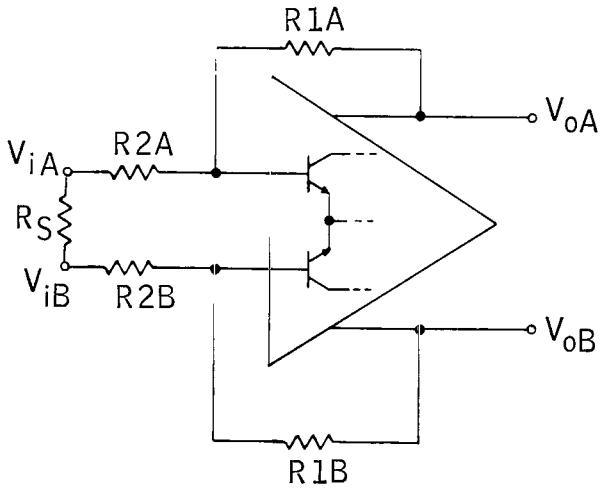


Figure A-3. - Overall base feedback.

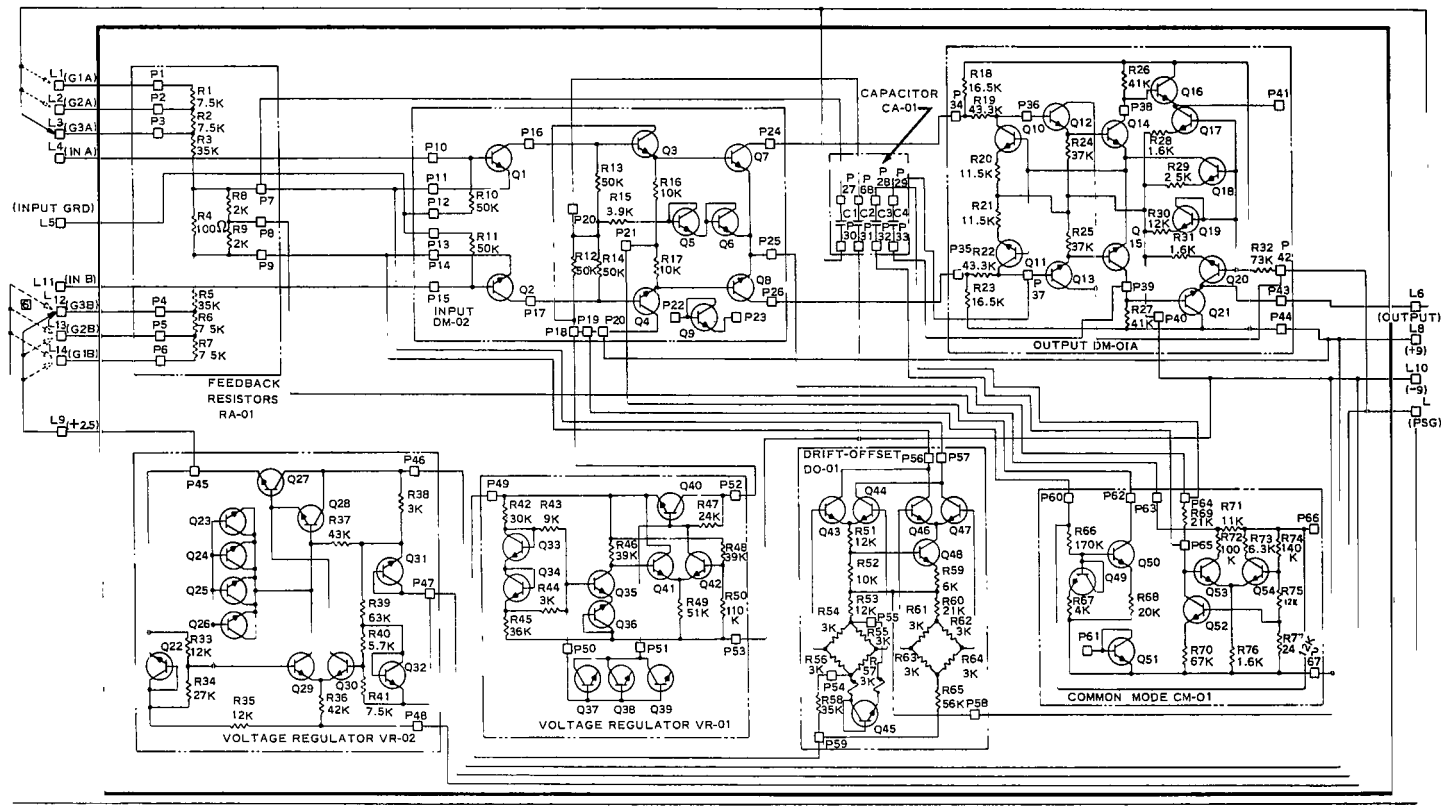


Figure A-4. - Complete amplifier.

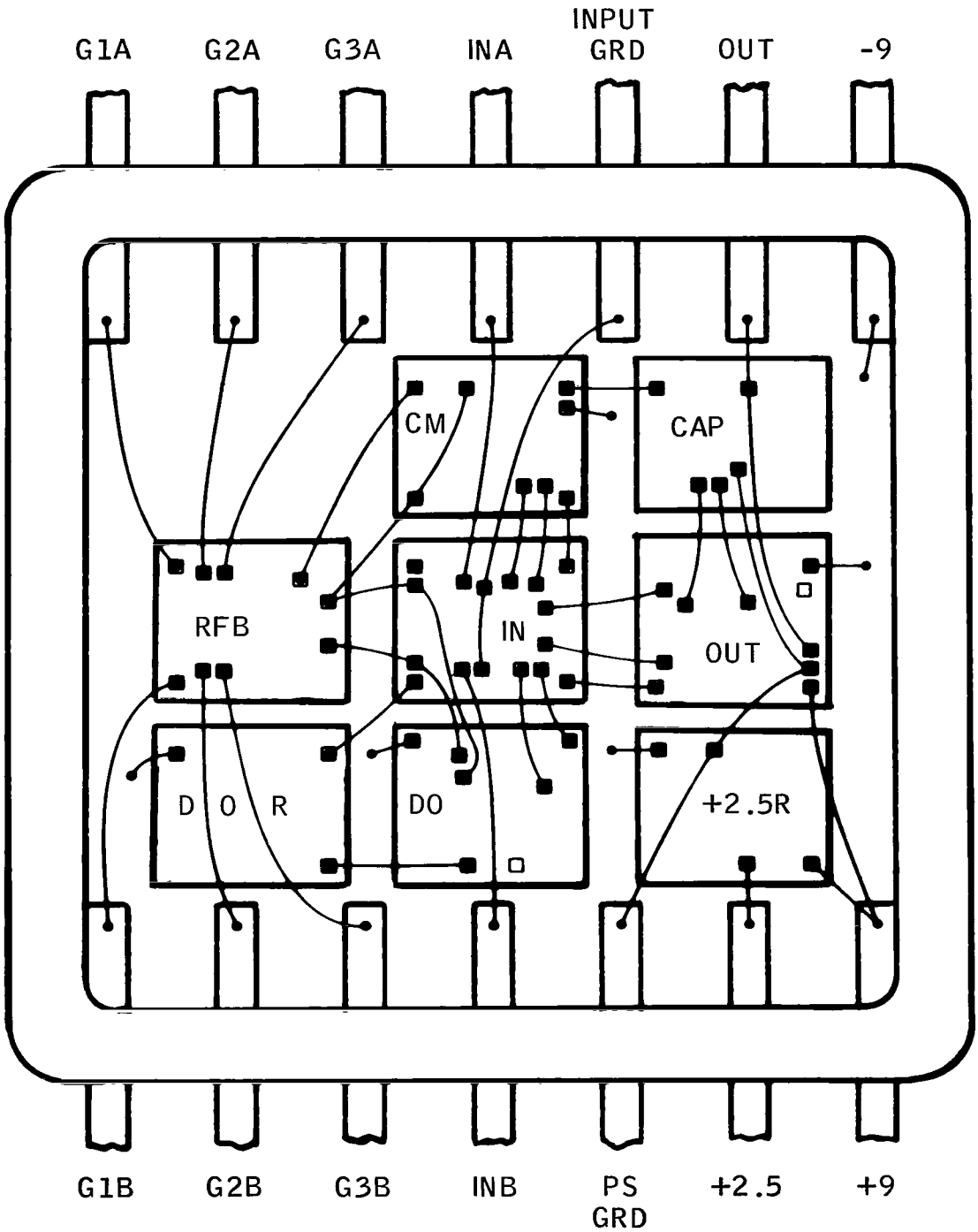


Figure A-5. - Package layout.

APPENDIX B

SPECIFICATIONS FOR A MICROMINIATURE dc AMPLIFIER

Scope

This specification covers one type of signal-conditioning module.

Applicable Documents

Interference Control Requirements, MIL-I-26600.

Requirements

Materials. - Except as specified herein, the selection of materials shall be the option of the contractor.

Design. - The module shall be designed to condition signals from sensors or similar devices to a level of 0 to +5 V for telemetering space program signals.

Construction. - Except as specified herein, the methods and techniques of construction shall be at the option of the contractor. The module shall be in a rectilinear configuration with weldable and solderable leads brought out in one plane.

Environmental specifications. - The module shall operate within the electrical specifications for any combination of the following environmental conditions.

Supply voltage conditions: The nominal voltage and current is to be selected by the contractor. This voltage may vary by ±5 percent over a frequency range of from dc to 100 kc.

Radio-frequency interference: The module shall meet Specification MIL-I-26600.

Temperature range: The module shall start and operate at any constant or variable (20° F/min maximum) temperature from -30° to +200° F. The module shall not be damaged when subjected to a nonoperating storage of at least 6 hours at any temperature from -65° to +250° F.

Service life: The module shall be capable of operating for a minimum of 2000 hours, continuously or otherwise, during a service life of 1 year.

Warmup time: The module shall be capable of operation with a warmup time not to exceed 50 μsec.

Electrical specifications. - The module shall operate within the following specifications when subjected to the environments specified.

Input signal: The module shall be capable of receiving variable differential input signals of from 0 to ±5 V without damage.

Input impedance: The input impedance shall be 50 kΩ or greater for any gain setting and for any frequency from dc to 5000 cps. A back current, not exceeding 0.2 μA, shall be supplied internally to accommodate a floating source.

Output bias and offset: With a zero input signal from a floating source impedance of from 0 to 375 Ω, the module output shall be capable of being set to 0 or 2.5 V. Selection shall be by moving jumper wires between external leads. This output voltage shall be within ±50 mV of the ideal value over the environment range specified.

Output signal: The module shall be capable of delivering output signals of from 0 to +5 V with the output bias set at either 0 or +2.5 V to a load of 50 kΩ to open circuit.

Output impedance: The output impedance of the module shall not exceed 100 Ω from dc to 5000 cps.

Voltage gain: The voltage gain shall be adjustable in steps within 1 percent of the ideal values of 700, 850, and 1000. This adjustment shall consist of jumper wires connected between identified leads. No components shall be added to change from one gain setting to another.

Gain stability and frequency response: The gain of the module shall be within ±1 percent of the dc value at 75° F from dc to 5000 cps. The frequency response shall not change more than ±1 percent over the specified environment range.

Output ripple: The maximum output ripple voltage shall be 25 mV peak to peak from dc through 15 mHz with 90-percent confidence level measured over a period of 1 second.

Linearity: The module shall have a linear output with ±12.5 mV of a straight line between the end points (nominal 0 and +5 V) with the output bias set at either 0 or +2.5 V.

Grounding procedure: The signal input shall be of the differential type and shall accommodate a floating source. No external input ground reference shall be needed.

Common mode: The module shall have a common mode rejection ratio of 80 dB or more for a 0- to 375-Ω floating source resistance for frequencies from dc to 5000 cps and for voltages of ±1.0 V.

Mechanical specifications. -

Volume: The module volume shall be 0.01 cu in. or less.

Color: The module case shall be opaque.

Product marking: The module and all external leads shall be marked for identification purposes in a permanent manner.

Workmanship: Uniformity of shapes, dimensions, and performances shall provide interchangeability of the complete module. There shall be no cracks, breaks, dents, or any other defects.

REFERENCES

1. Middlebrook, R. D.: Differential Amplifiers: Their Analysis and Their Applications in Transistor d. c. Amplifiers. John Wiley and Sons, Inc., 1963.

2. Middlebrook, R. D.: Design-Oriented Analysis of Feedback Amplifiers. Paper presented at National Electronics Conference (Chicago, Ill.), Oct. 1964.

3. Middlebrook, R. D.; and Taylor, A. D.: Differential Amplifier with Regulator Achieves High Stability, Low Drift. Electronics, vol. 34, no. 30, July 1961, pp. 56-59.

4. Hoffait, A. H.; and Thornton, R. D.: Limitations of Transistor DC Amplifiers. Proc. IEEE, vol. 52, no. 2, Feb. 1964, pp. 179-184.

5. Tuszynski, A.: Correlation Between Base-Emitter Voltage and its Temperature Coefficient. Solid State Design, vol. 3, no. 7, July 1962, pp. 32-35.

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